

Domenic J. Forte

Department of Electrical and Computer Engineering
216 Larsen Hall, P.O. Box 116200
University of Florida, Gainesville, FL 32611-6200
Phone: 352-392-1525 E-mail: dforte@ece.ufl.edu

RESEARCH INTERESTS

Counterfeit Electronic Component Detection and Avoidance: Includes physical inspection, electrical tests, and sensor design; provenance and supply chain tracking; from device level to system level

Physically Unclonable Functions (PUFs): Design, fabrication, and applications

Hardware Trojans: Pre-silicon prevention and post-silicon detection

Design Tools, Rules, Metrics, and Benchmarking: Hardware security assessment, mitigation, and obfuscation

Biometrics in IoT Applications: Includes emerging medico-chemical biometrics such as electrocardiogram (ECG) and photoplethysmograph (PPG)

PCB and IC Reverse and Anti-Reverse Engineering

Nanoscale Integration Challenges: 3D integration, thermal issues, security, and manufacturing variations in CMOS and beyond CMOS

EDUCATION

University of Maryland, College Park, MD

Ph.D., Electrical Engineering, August 2013

University of Maryland, College Park, MD

M.S., Electrical Engineering, December 2010

Manhattan College, Riverdale, NY

B.S., Electrical Engineering, *Summa Cum Laude*, May 2006

PROFESSIONAL EXPERIENCE

University of Florida, ECE Department, Gainesville, FL

FICS Research Security and Assurance (SCAN) Lab Director, August 2016 – present

Assistant Professor, July 2015 – present

University of Connecticut, ECE Department, Storrs, CT

Assistant Professor, August 2013 – July 2015

University of Maryland, ECE Department, College Park, MD

Research Assistant, June 2009 – August 2013

University of Maryland, ECE Department, College Park, MD

Teaching Assistant, August 2006 – December 2010

National Institutes of Health CIT DCB CBEL SPIS, Bethesda, MD

Co-op Student Intern, June 2007 – May 2009

Maryland Engineering Research Internship Teams (MERIT), College Park, MD

REU Student, Summer 2005

HONORS AND DISTINCTIONS

- UF Provost's Excellence Award for Assistant Professors, 2017–2018
- ACM TODAES Best Paper Award, 2018
- NSF Faculty Early Career Development (CAREER) Award, 2017
- International Symposium for Testing and Failure Analysis (ISTFA) Outstanding Paper Award, 2017
- International Joint Conference on Biometrics (IJCB) Best Student Paper Award, 2017
- ACM Computing Reviews Notable Computing Books and Articles – 2016, Hardware Category
- Army Research Office (ARO) Young Investigator Award, 2016
- IEEE International Symposium on Hardware Oriented Security and Trust (HOST) Best Paper Award, 2016
- IEEE International Symposium on Hardware Oriented Security and Trust (HOST) Best Paper Nomination ($\times 2$), 2016
- Schloss Dagstuhl - NSF Support Grant for Junior Researchers, Awarded, 2016
- IEEE International Symposium on Hardware Oriented Security and Trust (HOST) Best Paper Award, 2015
- Jacob K. Goldhaber Travel Award, University of Maryland, 2013
- Northrop Grumman Fellowship, 2012-2013 (Awarded to a top student in ECE)
- Design Automation Conference (DAC) Best Paper Nomination, 2012
- NASA/ESA Conference on Adaptive Hardware and Systems (AHS) Best Student Paper Award, 2011
- TA Teaching and Development (TATD) Fellow, University of Maryland, 2010–2011, 2011–2012
- George Corcoran Outstanding Teaching Award, University of Maryland, 2008 (Presented to two ECE graduate teaching assistants in 2008)
- Distinguished Teaching Assistant Award, University of Maryland, 2007-2008 (Awarded to top 10% of all graduate teaching assistants in the university)
- Co-recipient of medal for Electrical Engineering, Manhattan College, 2006 (Awarded at graduation to top two EE students in 2006)
- Next in Merit: Draddy Medal for General Excellence in Engineering, Manhattan College, 2006
- Society of Military Engineers (SAME) Scholarship, 2005
- Manhattan College Presidential Scholarship, 2002
- NY State Academic Excellence Scholarship, 2002

AWARDS RECEIVED BY STUDENT ADVISEES

- Ulbert (Joey) Botero: NSF Graduate Research Fellowship Program (GRFP) Awardee, 2018
- Sreeja Chowdury: Awarded second place in poster competition at the Second Workshop for Women in Hardware and Systems Security (WISE), 2018

- Ulbert (Joey) Botero: Awarded best poster at FICS Research Annual Conference on Cybersecurity 2018
- Nima Karimian: Awarded best student paper at International Joint Conference on Biometrics (IJCB) 2017
- Zimu Guo: Awarded best demo at FICS Research Annual Conference on Cybersecurity 2017
- Sreeja Chowdury: Awarded best hardware primitive poster at FICS Research Annual Conference on Cybersecurity 2017
- Zimu Guo and Nima Karimian: Awarded best hardware security poster at FICS Research Annual Conference on Cybersecurity 2016

BOOKS

- B1. M. Tehranipoor, **D. Forte**, G. Rose, S. Bhunia, “Security Opportunities in Nano Devices and Emerging Technologies”, CRC Press, 2017. *[Edited and Contributed]*
- B2. **D. Forte**, S. Bhunia, M. Tehranipoor, “Hardware Protection through Obfuscation”, Springer, 2017. *[Edited and Contributed]*
- B3. M. Tehranipoor, U. Guin, **D. Forte**, “Counterfeit Integrated Circuits: Detection and Avoidance”, Springer, 2015. *[Authored]*

BOOK CHAPTERS

- BC1. Q. Shi, **D. Forte**, M. Tehranipoor, “Deterrent Approaches Against Hardware Trojan Insertion,” in The Hardware Trojan War by Swarup Bhunia, and Mark M. Tehranipoor, Springer, 2018.
- BC2. F. Rahman, A. Nath, **D. Forte**, S. Bhunia, and M Tehranipoor, “Nano CMOS Logic-Based Security Primitive Design”, in Security Opportunities in Nano Devices and Emerging Technologies by Mark M. Tehranipoor, Domenic Forte, Garrett Rose, and Swarup Bhunia, CRC Press, 2017.
- BC3. H.T. Shen, F. Rahman, M. Tehranipoor, **D. Forte**, “Carbon-Based Novel Devices for Hardware Security”, in Security Opportunities in Nano Devices and Emerging Technologies by Mark M. Tehranipoor, Domenic Forte, Garrett Rose, and Swarup Bhunia, CRC Press, 2017.
- BC4. F. Rahman, A. Nath, S. Bhunia, **D. Forte**, M. Tehranipoor, “Composition of Physical Unclonable Functions: From Device to Architecture”, in Security Opportunities in Nano Devices and Emerging Technologies by Mark M. Tehranipoor, Domenic Forte, Garrett Rose, and Swarup Bhunia, CRC Press, 2017.
- BC5. B. Shakya, X. Xu, N. Asadi, M. Tehranipoor, **D. Forte**, “Leveraging Circuit Edit for Low-Volume Trusted Nanometer Fabrication”, in Security Opportunities in Nano Devices and Emerging Technologies by Mark M. Tehranipoor, Domenic Forte, Garrett Rose, and Swarup Bhunia, CRC Press, 2017.
- BC6. B. Shakya, M. Tehranipoor, S. Bhunia, **D. Forte**, “Introduction to Hardware Obfuscation: Motivation, Methods and Evaluation,” in Hardware Protection through Obfuscation by Domenic Forte, Swarup Bhunia, and Mark M. Tehranipoor, Springer, 2017.

- BC7. Z. Guo, M. Tehranipoor, **D. Forte**, “Permutation-Based Obfuscation,” in *Hardware Protection through Obfuscation by Domenic Forte, Swarup Bhunia, and Mark M. Tehranipoor*, Springer, 2017.
- BC8. M. T. Rahman, **D. Forte**, M. Tehranipoor, “Protection of Assets from Scan Chain Vulnerabilities through Obfuscation,” in *Hardware Protection through Obfuscation by Domenic Forte, Swarup Bhunia, and Mark M. Tehranipoor*, Springer, 2017.
- BC9. Q. Shi, K. Xiao, **D. Forte**, M. Tehranipoor, “Obfuscated Built-in Self Authentication,” in *Hardware Protection through Obfuscation by Domenic Forte, Swarup Bhunia, and Mark M. Tehranipoor*, Springer, 2017.
- BC10. A. Nahiyani, K. Xiao, **D. Forte**, M. Tehranipoor, “Security Rule Check,” in *Hardware IP Security and Trust by Prabhat Mishra, Swarup Bhunia and Mark Tehranipoor*, Springer, 2017.
- BC11. Q. Shi, **D. Forte**, M. Tehranipoor, “Analyzing Circuit Layout to Probing Attack,” in *Hardware IP Security and Trust by Prabhat Mishra, Swarup Bhunia and Mark Tehranipoor*, Springer, 2017.
- BC12. K. Xiao, **D. Forte**, M. Tehranipoor, “Circuit Timing Signature (CTS) for Detection of Counterfeit Integrated Circuits,” in *Secure System Design and Trustable Computing*, by Chip Hong Chang and Miodrag Potkonjak, Springer, 2016.

PEER-REVIEWED JOURNAL PUBLICATIONS (ACCEPTED)

- J1. A. Nahiyani, F. Farahmandi, P. Mishra, **D. Forte**, M. Tehranipoor, “Security-aware FSM Design Flow for Identifying and Mitigating Vulnerabilities to Fault Attacks”, to appear *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2018.
- J2. S. Amir, B. Shakya, X. Xu, Y. Jin, S. Bhunia, M. Tehranipoor, **D. Forte**, “Development and Evaluation of Hardware Obfuscation Benchmarks”, to appear *Journal of Hardware and Systems Security (HaSS)*, 2018.
- J3. Z. Guo, X. Xu, M. Tehranipoor, **D. Forte**, “SCARe: An SRAM-based Countermeasure Against IC Recycling Framework”, *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, Vol. 26., No. 4, April 2018.
- J4. M.M. Alam, S. Chowdhury, B. Park, D. Munzer, N. Maghari, M. Tehranipoor, **D. Forte**, “Challenges and Opportunities in Analog and Mixed Signal (AMS) Integrated Circuit (IC) Security”, *Journal of Hardware and Systems Security (HaSS)*, Vol. 2, No. 1, March 2018.
- J5. K. Yang, **D. Forte**, M. Tehranipoor, “ReSC: An RFID-Enabled Solution for Defending IoT Supply Chain”, *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, Vol. 23, No. 3, February 2018.
- J6. K. Yang, H. Shen, **D. Forte**, S. Bhunia, M. Tehranipoor, “Hardware-Enabled Pharmaceutical Supply Chain Security”, *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, Vol. 23, No. 3, January 2018.
- J7. F. Rahman, B. Shakya, Bicky, X. Xu, **D. Forte**, M. Tehranipoor, “Security Beyond CMOS: Fundamentals, Applications, and Roadmap”, *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, Vol. 25, No. 12, December 2017.

- J8. H. Shen, F. Rahman, B. Shakya, X. Xu, M. Tehranipoor, **D. Forte**, “Poly-Si Based Physical Unclonable Functions”, *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, Vol. 25, No. 11, November 2017.
- J9. E.L. Principe, N. Asadi, **D. Forte**, M. Tehranipoor, R. Chivas, M. DiBattista, S. Silverman, “Plasma FIB Deprocessing of Integrated Circuits from the Backside”, *Electronic Device Failure Analysis (EDFA)*, Vol. 19, No. 4, November 2017.
- J10. M.T. Rahman, A. Hosey, Z. Guo, J. Carroll, **D. Forte**, M. Tehranipoor, “Systematic Correlation and Cell Neighborhood Analysis of SRAM-PUF for Robust and Unique Key Generation,” *Journal of Hardware and Systems Security (HaSS)*, Vol. 1, No. 2, October 2017.
- J11. H. Wang, Q. Shi, **D. Forte**, M. Tehranipoor, “Probing Attacks on Integrated Circuits: Challenges and Research Opportunities”, *IEEE Design & Test*, Vol. 34, No. 5, October 2017.
- J12. N. Karimian, Z. Guo, M. Tehranipoor, **D. Forte**, “Highly Reliable Key Generation from Electrocardiogram (ECG),” *IEEE Transactions on Biomedical Engineering (TBME)*, Vol. 64, No. 6, June 2017.
- J13. U. Guin, S. Bhunia, **D. Forte**, M. Tehranipoor, “SMA: A System-Level Mutual Authentication for Protecting Electronic Hardware and Firmware,” *IEEE Transactions on Dependable and Secure Computing (TDSC)*, Vol. 14, No. 3, May-June 1 2017.
- J14. Z. Guo, J. Di, M. Tehranipoor, **D. Forte**, “Obfuscation based Protection Framework Against Printed Circuit Boards Privacy Violation,” *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, Vol. 22, No. 3, April 2017.
- J15. K. Yang, **D. Forte**, M. Tehranipoor, “CDTA: A Comprehensive Solution for Counterfeit Detection, Traceability and Authentication in IoT Supply Chain,” *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, Vol. 22, No. 3, April 2017.
- J16. B. Shakya, T. He, H. Salmani, **D. Forte**, S. Bhunia, M. Tehranipoor, “Benchmarking of Hardware Trojans and Maliciously Affected Circuits”, *Journal of Hardware and Systems Security (HaSS)*, Vol. 1, No. 1, April 2017.
- J17. M. Alam, H. Shen, N. Asadi, M. Tehranipoor, **D. Forte**, “Impact of X-ray Tomography on the Reliability of Integrated Circuits”, *IEEE Transactions on Device and Materials Reliability (TDMR)*, Vol. 17, No. 1, March 2017.
- J18. N. Asadi, M. Tehranipoor, **D. Forte**, “PCB Reverse Engineering Using Non-destructive X-ray Tomography and Advanced Image Processing”, *IEEE Transactions on Components, Packaging and Manufacturing (CPMT)*, Vol. 7, No. 2, Feb. 2017.
- J19. K. Xiao, **D. Forte**, Y. Jin, R. Karri, S. Bhunia, M. Tehranipoor, “Hardware Trojans: Lessons Learned After One Decade of Research”, *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, Vol. 22, No. 1, June 2016. [2018 ACM TODAES Best Paper, ACM Computing Reviews Notable Computing Books and Articles – 2016, Hardware Category]
- J20. U Guin, Q. Shi, **D. Forte**, M. Tehranipoor, “FORTIS: A Comprehensive Solution for Establishing Forward Trust for Protecting IPs and ICs,” *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, Vol. 21, No. 4, June 2016

- J21. U. Guin, **D. Forte**, M. Tehranipoor, “Design of Accurate Low-Cost On-Chip Structures for protecting Integrated Circuits against Recycling,” *IEEE Transactions on VLSI Systems (TVLSI)*, Vol. 24, No. 4, April 2016.
- J22. S. E. Quadir, J. Chen, **D. Forte**, N. Asadizanjani, S. Shahbazmohamadi, L. Wang, J. Chandy, M. Tehranipoor, “A Survey on Chip to System Reverse Engineering,” *ACM Journal on Emerging Technologies in Computing Systems (JETC)*, Vol. 13, No. 1, April 2016.
- J23. C. Bao, **D. Forte**, A. Srivastava, “On Reverse Engineering-Based Hardware Trojan Detection,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 35, No.1, Jan. 2016
- J24. C. Bao, **D. Forte**, A. Srivastava, “Temperature Tracking: Towards Robust Run-time Detection of Hardware Trojans,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)* Vol. 34, No. 10, Oct. 2015.
- J25. M.T. Rahman, F. Rahman, **D. Forte**, M. Tehranipoor, “An Aging-Resistant RO-PUF for Reliable Key Generation,” *IEEE Transactions on Emerging Topics in Computing (TETC)*, Sept. 2015.
- J26. A. Mazady, M.T. Rahman, **D. Forte**, M. Anwar, “Memristor Nano-PUF A Security Primitive: Theory and Experiment,” *IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS)*, Vol. 5, No. 2, June 2015.
- J27. K. Xiao, **D. Forte**, M. Tehranipoor, “A Novel Built-In Self Authentication Technique to Prevent Inserting Hardware Trojans,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 32, No. 12, Nov. 2014.
- J28. **D. Forte** and A. Srivastava, “Improving the Quality of Delay-based PUFs via Optical Proximity Correction,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 32, No. 12, Dec. 2013.
- J29. **D. Forte** and A. Srivastava, “Thermal-Aware Sensor Scheduling for Distributed Estimation,” *ACM Transactions on Sensor Networks (TOSN)*, Vol. 9, No. 4, July 2013.
- J30. **D. Forte** and A. Srivastava, “Energy and Thermal-Aware Video Coding via Encoder/Decoder Workload Balancing”, *IEEE Transactions on Embedded Computing Systems (TECS)*, Vol. 12, No. 2, May 2013.
- J31. **D. Forte** and A. Srivastava, “Resource-Aware Architectures for Adaptive Particle Filter Based Visual Target Tracking”, *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, Vol. 18, No. 2, April 2013.

PEER-REVIEWED CONFERENCE/WORKSHOP PUBLICATIONS

- C1. J. Park, X. Xu, Y. Jin, **D. Forte**, M. Tehranipoor, “Power-based Side-Channel Instruction-level Disassembler”, to appear *Design Automation Conference (DAC)*, June 2018.
- C2. S. Chowdhury, X. Xu, M. Tehranipoor, **D. Forte**, “Aging Resistant RO PUF with Increased Reliability in FPGA”, *International Conference on Reconfigurable Computing and FPGAs (ReConFig)*, Dec. 2017.
- C3. E.L. Principe, N.Asadizanjani, **D. Forte**, M. Tehranipoor, R. Chivas, M. DiBattista, S. Silverman, M. Marsh, N. Piche, J. Mastovich, “Steps Toward Automated Deprocess-

- ing of Integrated Circuits,” *International Symposium for Testing and Failure Analysis (ISTFA)*, Nov. 2017. [**ISTFA 2017 Outstanding Paper Award**]
- C4. A. Chhotaray, A. Nahiyani, T. Shrimpton, **D. Forte**, M. Tehranipoor, “Standardizing Bad Cryptographic Practice - A Teardown of the IEEE Standard for Protecting Electronic-Design Intellectual Property,” *ACM Conference on Computer and Communications Security (CCS)*, Nov. 2017.
- C5. Z. Guo, X. Xu, M. Tehranipoor, **D. Forte**, “MPA: Model-assisted PCB Attestation via Board-level RO and Temperature Compensation”, *IEEE Asian Hardware-Oriented Security and Trust (AsianHOST)*, Oct. 2017.
- C6. K. Yang, U. Botero, H. Shen, **D. Forte**, M. Tehranipoor, “A Split Manufacturing Approach for Unclonable Chipless RFIDs for Pharmaceutical Supply Chain Security”, *IEEE Asian Hardware-Oriented Security and Trust (AsianHOST)*, Oct. 2017.
- C7. A. Nahiyani, M. Sadi, R. Vittal, G. Contreras, **D. Forte**, M. Tehranipoor, “Hardware Trojan Detection through Information Flow Security Verification,” *IEEE International Test Conference (ITC)*, Oct. 2017.
- C8. N. Karimian, D. Woodard, **D. Forte**, “On the Vulnerability of ECG Verification to Online Presentation Attacks,” *IEEE International Joint Conference on Biometrics (IJCB)*, Oct. 2017. [**IJCB 2017 Best Student Paper Award**]
- C9. X. Xu, B. Shakya, M. Tehranipoor, **D. Forte**, “Novel Bypass Attack and BDD-based Tradeoff Analysis Against all Known Logic Locking Attacks,” *International Conference on Cryptographic Hardware and Embedded Systems (CHES)*, Sept. 2017.
- C10. Z. Guo, X. Xu, M. Tehranipoor, **D. Forte**, “FFD: A Framework for Fake Flash Detection”, *Design Automation Conference (DAC)*, June 2017.
- C11. Q. Shi, K. Xiao, **D. Forte**, M. Tehranipoor, “Securing Split Manufactured ICs with Wire Lifting Obfuscated Built-In Self-Authentication”, *GLSVLSI*, May 2017.
- C12. S. Amir, B. Shakya, **D. Forte**, M. Tehranipoor, S. Bhunia, “Comparative Analysis of Hardware Obfuscation for IP Protection”, *GLSVLSI*, May 2017.
- C13. T. Byrant, S. Chowdhury, **D. Forte**, M. Tehranipoor, N. Maghari, “A Stochastic All-Digital Weak Physically Unclonable Function for Analog/Mixed-Signal Applications”, *Hardware-Oriented Security and Trust (HOST)*, May 2017
- C14. N. Karimian, F. Tehranipoor, Z. Guo, M. Tehranipoor, **D. Forte**, “Noise Assessment Framework for Optimizing ECG Key Generation”, *IEEE International Conference on Technologies for Homeland Security (HST)*, April 2017.
- C15. N. Karimian, Z. Guo, M. Tehranipoor, **D. Forte**, “Human Recognition from Photo-plethysmography (PPG) Based on Non-fiducial Features”, *IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP)*, March 2017.
- C16. N. Karimian, M. Tehranipoor, **D. Forte**, “Non-Fiducial PPG-based Authentication for Healthcare Application”, *International Conference on Biomedical and Health Informatics (BHI)*, February 2017.
- C17. G. K. Contreras, A. Nahiyani, S. Bhunia, **D. Forte**, M. Tehranipoor, “Security Vulnerability Analysis of Design-for-Test Exploits for Asset Protection in SoCs,” *Asia and South Pacific Design Automation Conference (ASP-DAC)*, Jan. 2017.

- C18. Z. Guo, M. Tehranipoor, **D. Forte**, “Aging Attacks for Key Extraction on Permutation-Based Obfuscation,” *IEEE Asian Hardware-Oriented Security and Trust (AsianHOST)*, Dec. 2016.
- C19. T. Rahman, **D. Forte**, X. Wang, M. Tehranipoor, “Enhancing Noise Sensitivity of Embedded SRAMs for Robust True Random Number Generation in SoCs,” *IEEE Asian Hardware-Oriented Security and Trust (AsianHOST)*, Dec. 2016.
- C20. M. M. Alam, M. Tehranipoor, **D. Forte** “Recycled FPGA Detection Using Exclusive LUT Path Delay Characterization,” *IEEE International Test Conference (ITC)*, Nov. 2016.
- C21. B. Shakya, N. Asadi, **D. Forte**, M. Tehranipoor, “Chip Editor: Leveraging Circuit Edit for Logic Obfuscation and Trusted Fabrication,” *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Nov. 2016.
- C22. Z. Guo, B. Shakya, H. Shen, S. Bhunia, N. Asadizanjani, **D. Forte**, M. Tehranipoor, “A New Methodology to Protect PCBs from Non-destructive Reverse Engineering,” *International Symposium for Testing and Failure Analysis (ISTFA)*, Nov. 2016.
- C23. N. Asadizanjani, **D. Forte**, M. Tehranipoor, “Non-destructive Bond Pull and Ball Shear Failure Analysis Based on Real Structural Properties” *International Symposium for Testing and Failure Analysis (ISTFA)*, Nov. 2016.
- C24. N. Asadizanjani, S. Gattigowda, N. Dunn, M. Tehranipoor, **D. Forte**, “A Database for Counterfeit Electronics and Automatic Defect Detection Based on Image Processing and Machine Learning,” *International Symposium for Testing and Failure Analysis (ISTFA)*, Nov. 2016.
- C25. T. Bryant, S. Chowdhury, **D. Forte**, M. Tehranipoor, N. Maghari, “A Stochastic Approach to Analog Physical Unclonable Function,” *IEEE Midwest Symposium on Circuits and Systems (MWSCAS)*, Oct. 2016.
- C26. N. Karimian, M. Tehranipoor, D. Woodard, **D. Forte**, “Biometrics for Authentication in Resource-Constrained Systems,” *International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC)*, August 2016.
- C27. H. Shen, F. Rahman, B. Shakya, M. Tehranipoor, **D. Forte**, “Selective Enhancement of Randomness at the Materials Level: Poly-Si Based Physical Unclonable Functions (PUFs)”, *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, July 2016.
- C28. A. Nahiyani, K. Xiao, K. Yang, Y. Jin, **D. Forte**, M. Tehranipoor, “AVFSM: A Framework for Identifying and Mitigating Vulnerabilities in FSMs”, *Design Automation Conference (DAC)*, June 2016.
- C29. Z. Guo, N. Karimian, M. Tehranipoor, **D. Forte**, “Hardware Security Meets Biometrics for the Age of IoT”, *IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2016.
- C30. T. Le, J. Di, M. Tehranipoor, **D. Forte**, L. Wang, “Tracking Data Flow at Gate-Level through Structural Checking”, *GLSVLSI*, May 2016.
- C31. Q. Shi, N. Asadizanjani, **D. Forte**, M. Tehranipoor, “A Layout-driven Framework to Assess Vulnerability of ICs to Microprobing Attacks”, *Hardware-Oriented Security and Trust (HOST)*, May 2016. [**HOST 2016 Best Paper Award**]

- C32. Z. Guo, M. T. Rahman, M. Tehranipoor, **D. Forte**, “A Zero-cost Approach to Detect Recycled SoCs Using Embedded SRAM”, *Hardware-Oriented Security and Trust (HOST)*, May 2016.
- C33. K. Yang, **D. Forte**, M. Tehranipoor, “UCR: Unclonable Chipless RFID Tag”, *Hardware-Oriented Security and Trust (HOST)*, May 2016. [**HOST 2016 Best Paper Nomination**]
- C34. F. Rahman, **D. Forte**, and Mark Tehranipoor, “Reliability vs. Security: Challenges and Opportunities for Developing Reliable and Secure Integrated Circuits,” *International Reliability Physics Symposium (IRPS)*, April 2016
- C35. B. Shakya, F. Rahman, M. Tehranipoor, **D. Forte**, “Harnessing Nanoscale Device Properties for Hardware Security”, *Microprocessor Test and Verification (MTV)*, Dec. 2015.
- C36. K. Yang, **D. Forte**, and M. Tehranipoor, “Protecting Endpoint Devices in IoT Supply Chain”, *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Nov. 2015.
- C37. H. Dogan, M. Alam, N. Asadizanjani, S. Shahbazmohamadi, **D. Forte**, and M. Tehranipoor, “Analyzing the Impact of X-ray Tomography for Non-destructive Counterfeit Detection”, *International Symposium for Testing and Failure Analysis (ISTFA)*, Nov. 2015.
- C38. N. Asadizanjani, S. Shahbazmohamadi, M. Tehranipoor, **D. Forte** “Non-destructive PCB Reverse Engineering Using X-ray Micro Computed Tomography”, *International Symposium for Testing and Failure Analysis (ISTFA)*, Nov. 2015.
- C39. B. Shakya, U. Guin, M. Tehranipoor, **D. Forte**, “Performance Optimization for On-Chip Sensors to Detect Recycled ICs,” *IEEE International Conference on Computer Design (ICCD)*, Oct. 2015.
- C40. M. T. Rahman, **D. Forte**, F. Rahman, M. Tehranipoor, “A Pair Selection Algorithm for Robust RO-PUF Against Environmental Variations and Aging,” *IEEE International Conference on Computer Design (ICCD)*, Oct. 2015.
- C41. S. Chen, J. Chen, **D. Forte**, J. Di, M. Tehranipoor, L. Wang, “Chip-level Anti-reverse Engineering using Transformable Interconnects,” *IEEE Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT)*, Oct. 2015.
- C42. K. Yang, **D. Forte**, M. Tehranipoor, “ReSC: RFID-enabled Supply Chain Management and Traceability for Network Devices,” *11th Workshop on RFID Security (RFIDSec 2015)*, June 2015.
- C43. Z. Guo, J. Di, M. Tehranipoor, **D. Forte**, “Investigation of Obfuscation-based Anti-Reverse Engineering for Printed Circuit Boards,” *Design Automation Conference (DAC) 2015*, June 2015.
- C44. K. Xiao, **D. Forte**, M. Tehranipoor, “Efficient and Secure Split Manufacturing via Obfuscated Built-In Self-Authentication,” *Hardware-Oriented Security and Trust (HOST) 2015*, May 2015. [**HOST 2015 Best Paper Award**]
- C45. N. Karimian, F. Tehranipoor, M.T. Rahman, **D. Forte**, “Genetic Algorithm for Hardware Trojan Detection with Ring Oscillator Network (RON)” in *IEEE International Conference on Technologies for Homeland Security (HST)*, April 2015.

- C46. K. Yang, **D. Forte**, M. Tehranipoor, “An RFID-based Technology for Electronic Component and System Counterfeit Detection and Traceability” in *IEEE International Conference on Technologies for Homeland Security (HST)*, April 2015.
- C47. A. Hosey, M.T. Rahman, K. Xiao, **D. Forte**, M. Tehranipoor, “Advanced Analysis of Cell Stability for Reliable SRAM PUF,” *IEEE Asian Test Symposium (ATS)*, Nov. 2014.
- C48. S. Shahbazmohamadi, **D. Forte**, M. Tehranipoor, “Advanced Physical Inspection Methods for Counterfeit Detection”, *International Symposium for Testing and Failure Analysis (ISTFA)*, Nov. 2014.
- C49. M.T. Rahman, **D. Forte**, Q. Shi, G. Contreras, M. Tehranipoor, “CSST: Preventing Distribution of Unlicensed and Rejected ICs by Untrusted Foundry and Assembly,” *IEEE Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT)*, Oct. 2014.
- C50. H. Dogan, **D. Forte**, M. Tehranipoor, “Aging Analysis for Recycled FPGA Detection,” *IEEE Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT)*, Oct. 2014.
- C51. U. Guin, X. Zhang, **D. Forte**, M. Tehranipoor, “Low-cost On-Chip Structures for Combating Die and IC Recycling,” *Design Automation Conference (DAC)*, June 2014.
- C52. M.T. Rahman, K. Xiao, X. Zhang, **D. Forte**, Z. Shi, M. Tehranipoor, “TI-TRNG: Technology Independent True Random Number Generator,” *Design Automation Conference (DAC)*, June 2014.
- C53. M.T. Rahman, **D. Forte**, Q. Shi, G. Contreras, M. Tehranipoor, “CSST: An Efficient Secure Split-Test for Preventing IC Piracy,” in *IEEE North Atlantic Test Workshop (NATW)*, May 2014
- C54. K. Xiao, M.T. Rahman, **D. Forte**, M. Su, Y. Huang, M. Tehranipoor, “Bit Selection Algorithm Suitable for High-Volume Production of SRAM-PUF,” *Hardware-Oriented Security and Trust (HOST)*, May 2014.
- C55. C. Bao, **D. Forte**, A. Srivastava, “On Application of One-class SVM to Reverse Engineering-Based Hardware Trojan Detection”, in *International Symposium on Quality Electronic Design (ISQED)*, March 2014.
- C56. M.T. Rahman, **D. Forte**, J. Fahrny, M. Tehranipoor, “ARO-PUF: An Aging-Resistant Ring Oscillator PUF Design”, in *Design, Automation, and Test in Europe (DATE)*, March 2014.
- C57. U. Guin, **D. Forte**, M. Tehranipoor, “Anti-Counterfeit Techniques: From Design to Resign”, in *Microprocessor Test and Verification (MTV)*, December 2013.
- C58. **D. Forte**, C. Bao, A. Srivastava, “Temperature Tracking: An Innovative Run-Time Approach for Hardware Trojan Detection”, *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, November 2013.
- C59. **D. Forte** and A. Srivastava, “Manipulating Manufacturing Variations for Better Silicon-Based Physically Unclonable Functions”, *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, August 2012.

- C60. **D. Forte** and A. Srivastava, “On Improving the Uniqueness of Silicon-Based Physically Unclonable Functions Via Optical Proximity Correction”, *Design Automation Conference (DAC)*, June 2012. [**DAC-2012 Best Paper Nomination**]
- C61. **D. Forte** and A. Srivastava, “Adaptable Architectures for Distributed Visual Target Tracking”, *IEEE International Conference on Computer Design (ICCD)*, October 2011.
- C62. **D. Forte** and A. Srivastava, “Energy-Aware and Quality-Scalable Data Placement and Retrieval for Disks in Video Server Environments”, *IEEE International Conference on Computer Design (ICCD)*, October 2011.
- C63. **D. Forte** and A. Srivastava, “Energy-aware video storage and retrieval in server environments,” *International Green Computing Conference and Workshops (IGCC)*, July 2011.
- C64. **D. Forte** and A. Srivastava, “Resource-aware architectures for particle filter based visual target tracking,” *International Green Computing Conference and Workshops (IGCC)*, July 2011.
- C65. **D. Forte** and A. Srivastava, “Adaptable video compression and transmission using lossy and workload balancing techniques”, *NASA/ESA Conference on Adaptive Hardware and Systems (AHS)*, June 2011. [**Awarded AHS-2011 Best Student Paper**]
- C66. **D. Forte** and A. Srivastava, “Energy-aware video coding of multiple views via workload balancing”, *NASA/ESA Conference on Adaptive Hardware and Systems (AHS)*, June 2011.
- C67. **D. Forte** and A. Srivastava, “Energy and Thermal-Aware Video Coding via Encoder/Decoder Workload Balancing”, *International Symposium on Low Power Electronics and Design (ISLPED)*, August 2010.
- C68. **D. Forte** and A. Srivastava, “Thermal-Aware Sensor Scheduling for Distributed Estimation”, *International Conference on Distributed Computing in Sensor Systems (DCOSS)*, June 2010.

NON-REFEREED CONFERENCE PAPERS

- CP1. E.L. Principe, N. Asadi, **D. Forte**, M. Tehranipoor, M. DiBattista, R. Chivas, S. Silverman, N. Piche, M. Marsh, J. Mastovich, “Steps Toward Computational Guided Deprocessing of Integrated Circuits” in *GOMACTech*, March 2018.
- CP2. D. Capecchi, G. Contreras, **D. Forte**, M.Tehranipoor, S. Bhunia, “Automated SoC Security from Design to Fabrication” in *GOMACTech*, March 2018.
- CP3. S. Baireddy, U.J. Botero, N. Asadi, M.Tehranipoor, D. Woodard, **D. Forte**, “Automated Detection of Counterfeit IC Defects Using Image Processing” in *GOMACTech*, March 2018.
- CP4. U.J. Botero, M.Tehranipoor, **D. Forte**, “Downgrade: A Framework for Obsolescence Handling through Backwards Compatibility” in *GOMACTech*, March 2018.
- CP5. Z. Guo, M. Tehranipoor, **D. Forte**, “Memory-based Counterfeit IC Detection Framework”, *SRC TECHCON*, September 2017.
- CP6. Q. Shi, N. Asadizanjani, **D. Forte**, M.Tehranipoor, “Layout-based Microprobing Vulnerability Assessment for Security Critical Applications,” in *GOMACTech*, March

2017.

- CP7. M. T. Rahman, **D. Forte**, and M. Tehranipoor, "SRAM Inspired Design and Optimization for Developing Robust Security Primitives," in *SRC TECHCON*, September 2016. [**Awarded Best in Session**]
- CP8. M. M. Alam, N. Asadizanjani, M. Tehranipoor, **D. Forte**, "The Impact of X-ray Tomography on the Reliability of FPGAs " in *GOMACTech*, March 2016.
- CP9. Z. Guo, N. Karimian, M. Tehranipoor, **D. Forte**, "Biometric Based Human-to-Device (H2D) Authentication", in *GOMACTech*, March 2016.
- CP10. N. Asadizanjani, S. Shahbazmohamadi, **D. Forte**, M. Tehranipoor, "Nondestructive X-ray Tomography Based Bond Pull and Ball Shear Analysis" in *GOMACTech*, March 2016.
- CP11. M. T. Rahman, **D. Forte**, and M. Tehranipoor, "Robust SRAM-PUF: Cell Stability Analysis and Novel Bit-Selection Algorithm," *SRC TECHCON*, September 2015.
- CP12. M.T. Rahman, A. Hosey, F. Rahman, **D. Forte**, M. Tehranipoor, "RePa: A Pair Selection Algorithm for Reliable Keys from RO-based PUF" in *GOMACTech*, March 2015.
- CP13. H. Dogan, **D. Forte**, M. Tehranipoor, "Aging Analysis for Recycled FPGA Detection" in *GOMACTech*, March 2015.
- CP14. N. Asadizanjani, S. E. Quadir, S. Shahbazmohamadi, M. Tehranipoor, **D. Forte**, "Rapid Non-destructive Reverse Engineering of Printed Circuit Boards by High Resolution X-ray Tomography" in *GOMACTech*, March 2015.
- CP15. U. Guin, **D. Forte**, M. Tehranipoor, "Low-cost On-Chip Structures for Combatting Die and IC Recycling," in *GOMACTech*, March 2014.
- CP16. K. Xiao, M.T. Rahman, **D. Forte**, M. Tehranipoor, "Low-cost Analysis for Identification of Mass-Produced Electronic Devices," in *GOMACTech*, March 2014.
- CP17. U. Guin, **D. Forte**, D. DiMase, M. Tehranipoor, "Counterfeit IC Detection: Test Method Selection Considering Test Time, Cost, and Tier Level Risks," in *GOMACTech*, March 2014.

PATENTS

- Pt1. M. Tehranipoor, **D. Forte**, N. Asadizanjani, Q. Shi, *Layout-Driven Method to Assess Vulnerability of ICs To Microprobing Attacks*, filed December 2017.
- Pt2. M. Tehranipoor, K. Yang, H. Shen, **D. Forte**, *UCR: An Unclonable Environmentally-Sensitive Chipless RFID Tag*, filed October 2017.
- Pt3. M. Tehranipoor, **D. Forte**, B. Shakya, N. Asadizanjani, *Circuit Edit and Obfuscation for Trusted Chip Fabrication*, filed June 2017.
- Pt4. M. Tehranipoor, U. Guin, **D. Forte**, *A Comprehensive Framework for Protecting Intellectual Property in Semiconductor Industry*, filed June 2017.

ADVISEES

Current Post-doctoral Fellows and Research Scientists

Haoting Shen*, Jungmin Park*[†], Qihang Shi*

Past Post-doctoral Fellows and Research Scientists

Navid Asadi*

Current PhD

University of Florida: Zimu Guo, Bicky Shakya, Mahbub Alam, Sreeja Chowdhury, Sarah Amir, Ulbert (Joey) Botero, Sumaiya (Joyti) Shomaji, Muhtadi (Zaki) Choudhury

Past PhD (Title and Current Affiliation)

University of Connecticut: Nima Karimian (Assistant Professor, San Jose State University)

Past MS

University of Florida: Bicky Shakya, Rahul Vittal, Janani Prakash
University of Connecticut: Nima Karimianbahnemiri

Past Visiting MS (Institution)

Pallabi Ghosh (IIT Kharagpur)

Current Undergrad

James Mashburn

Past Undergrad

Sriram Baireddy, Jackson Carroll, Julia Merino-Calleja, Andrew Stern, Nathan Dunn*, Somtochukwu Okwuosah, Alison Hosey, Jacquelyn Khadijah-Hajdu*, Wesley Stevens*, Ryan Nesbit*, Dan Guerrero*, Shane Tobey*, Kasim Ward*, Carl DiFrederico*, Anthony Schend*, Michael Vetri*, Tyler Rich*

*Note: * and † indicate co-advised by Mark Tehranipoor and Swarup Bhunia respectively*

PROFESSIONAL ACTIVITIES

Editorial Activities

Associate Editor, Springer Journal of Hardware and System Security (HaSS), 2016–present

Guest Editor, Springer Journal of Hardware and System Security (HaSS) Special Issue on “Hardware Reverse Engineering and Obfuscation”, 2018

Guest Editor, IEEE Computer Special Issue on “Supply Chain Security for Cyber-Infrastructure”, 2016

Conference Organizing Committee

Vice Program Chair, International Symposium on Hardware-Oriented Security and Trust (HOST), 2018

Reverse Engineering Track Chair, International Symposium for Testing and Failure Analysis (ISTFA), 2018

Publicity Chair, Workshop on Attacks and Solutions in Hardware Security (ASHES), 2018
Publicity Chair, IEEE Asian Hardware-Oriented Security and Trust Symposium (Asian-HOST), 2016–2018
Program Co-Chair, International Verification and Security Workshop (IVSW), 2017
Tutorial Chair, International Symposium on Hardware-Oriented Security and Trust (HOST), 2017
Poster Chair, FICS Research Annual Conference on Cybersecurity, 2017
Reverse Engineering Track Chair, International Symposium for Testing and Failure Analysis (ISTFA), 2016
Publicity Chair, International Symposium on Hardware-Oriented Security and Trust (HOST), 2015, 2016
Hardware Security Challenge Co-Chair, CSI Cybersecurity, Education & Diversity Challenge Week (CyberSEED), 2014

Program Committee (PC)

2018: Asian Hardware Oriented Security and Trust Symposium (AsianHOST), DAC PhD Forum, Great Lakes Symposium on VLSI (GLSVLSI), International Symposium on Quality Electronic Design (ISQED), International Symposium on Hardware-Oriented Security and Trust (HOST), International Symposium for Testing and Failure Analysis (ISTFA), International Test Conference (ITC), International Workshop on Physical Attacks and Inspection on Electronics (PAINE), Network and Distributed System Security Symposium (NDSS), Smart Card Research and Advanced Application Conference (CARDIS)

2017: Asian Hardware Oriented Security and Trust Symposium (AsianHOST), DAC PhD Forum, Great Lakes Symposium on VLSI (GLSVLSI), International Conference on Computer-Aided Design (ICCAD), International Symposium on Hardware-Oriented Security and Trust (HOST), International Symposium on Quality Electronic Design (ISQED), International Test Conference (ITC), Network and Distributed System Security Symposium (NDSS), Smart Card Research and Advanced Application Conference (CARDIS), Workshop on Attacks and Solutions in Hardware Security (ASHES)

2016: Asian Hardware Oriented Security and Trust Symposium (AsianHOST), Design Automation Conference (DAC), DAC PhD Forum, International Symposium on Hardware-Oriented Security and Trust (HOST), International Conference on Computer-Aided Design (ICCAD), International Symposium on Quality Electronic Design (ISQED), International Symposium for Testing and Failure Analysis (ISTFA)

2015: Design Automation Conference (DAC), International Conference on Computer-Aided Design (ICCAD), International Conference on Computer Design (ICCD), International Symposium on Hardware-Oriented Security and Trust (HOST), International Test Conference (ITC), International Symposium on Quality Electronic Design (ISQED), Workshop on Embedded Systems Security (WESS)

2014: International Symposium on Hardware-Oriented Security and Trust (HOST), TRUDEVICE Workshop on Test and Fault Tolerance for Secure Devices, Workshop on Embedded Systems Security (WESS)

2013: Workshop on Embedded Systems Security (WESS)

Proposal Panelist/Reviewer

2018: National Science Foundation (NSF)

2017: American Association for the Advancement of Science (AAAS), Army Research Office (ARO)

2016: National Science Foundation (NSF)

Reviewer for

ACM Journal on Emerging Technologies in Computing Systems (JETC), 2015

ACM Transactions on Design Automation of Electronic Systems (TODAES), 2014-2016

ACM Transactions on Privacy and Security (TOPS), 2017

IEEE Access, 2015

IEEE Communications Letters, 2014

IEEE Design & Test, 2014

IEEE Journal of Solid-State Circuits, 2018

IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS), 2015

IEEE Transactions on Circuits and Systems I (TCAS1), 2014-2017

IEEE Transactions on Circuits and Systems II (TCAS2), 2014

IEEE Transactions on Computer-Aided Design of Integrated Circuits (TCAD), 2014, 2016-2017

IEEE Transactions on Computers, 2015-2017

IEEE Transactions on Embedded Computing Systems (TECS), 2016

IEEE Transactions on Emerging Topics in Computing (TETC), 2013, 2015

IEEE Transactions on Information Forensics and Security (TIFS), 2014-2017

IEEE Transactions on Multi-Scale Computing Systems (TMSCS), 2015

IEEE Transactions on Nanotechnology (TNANO), 2015

IEEE Transactions on Dependable and Secure Computing (TDSC), 2017

IEEE Transactions on VLSI Systems (TVLSI), 2013-2018

IET Computers & Digital Techniques, 2014

Image and Vision Computing, 2017

Journal of Electronic Testing: Theory and Applications (JETTA), 2016

Departmental Appointments

University of Florida, ECE Department, Gainesville, Fl

Faculty Search Committee, AY 2017-2018

Graduate Recruiting & Admissions Committee (GRAC), AY 2015-2016, AY 2016-2017, AY 2017-2018

EEL 3111 Circuits 1 ABET Course Committee, AY 2015-2016, AY 2016-2017

EEE 4310 Digital Integrated Circuits ABET Course Committee, AY 2015-2016, AY 2016-2017, AY 2017-2018

EEE 4404 Mixed Signal IC Testing I ABET Course Committee, AY 2016-2017, AY 2017-2018

EEL 4242 Power Electronics 1 ABET Course Committee, AY 2017-2018

University of Connecticut, ECE Department, Storrs, CT

Department Judge- First Annual Graduate Poster Competition, 2015

Course and Curriculum Committee, AY 2014-2015

Invited Talks (14)

- International Test & Evaluation Association 2018 Cybersecurity Workshop**, Fort Walton Beach, FL March 2018
Title: "Hardware for Cyber (H4C): A Suite of Electronic System Protections from Nano to System Levels"
- CIA Tech Exchange on Trust & Validation of Electronics**, Chantilly, VA Feb. 2018
Title: "Trust & Validation of Electronics at FICS Research"
- Cisco Research Center System and Platform Security PI Summit**, San Jose, CA Dec. 2017
Title: "Teardown and Recommendations for IEEE Standard for Protecting Electronic-Design Intellectual Property"
- International Test Conference (ITC) 2017**, Fort Worth, TX Nov. 2017
Title: "Upgrade/Downgrade: A Perspective on Challenges and Opportunities in Overcoming the Legacy System Issue"
- AsianHOST 2017**, Beijing, China Oct. 2017
Title: "Security of the Internet of Things: New Frontiers"
- GRC Technology Transfer e-Workshop**, WebEx July 2016
Title: "Design of Low-Cost Memory-Based Security Primitives and Techniques for High-Volume Products"
- Workshop on Cyber Science, Biometrics and Digital Forensics**, Miami, FL November 2015
Title: "Biometrics Meets Hardware Security"
- Northrop Grumman Lunch N Learn**, Baltimore, MD November 2015
Title: "New Directions in Hardware Security and Supply Chain Assurance"
- Workshop on Cryptography and Hardware Security for the Internet of Things**, College Park, MD October 2015
Title: "Hardware Security Challenges and Solutions in the IoT Era"
- University of Florida**, Gainesville, FL March 2015
Title: "Hardware-based Primitives for System Authentication and Protection"
- Design, Automation & Test in Europe (DATE)**, Dresden, DE March 2014
Title: "Protocol Attacks on Advanced PUF Protocols and Countermeasures"
- University of South Florida**, Tampa, FL March 2013
Title: "Towards Comprehensive Solutions for Hardware Security"
- Raytheon BBN Technologies**, Columbia, MD March 2013
Title: "Towards Comprehensive Solutions for Hardware Security"
- University of Connecticut**, Storrs, CT February 2013
Title: "Towards Comprehensive Solutions for Hardware Security"

Campus and Departmental Talks (6)

- Forum on Trusted and Assured MicroElectronics (TAME)**, Gainesville, FL November 2017
Title: "Emerging Solutions for Trusted and Assured Microelectronics"
- UF Eta Kappa Nu (HKN) Speaker Series**, Gainesville, FL November 2017
Title: "Introduction to FICS Research"
- FICS Annual Conference on Cybersecurity**, Gainesville, FL February 2016

Title: "Human-to-Device Authentication"

CHASE Conference on Secure/Trustworthy Systems and Supply Chain Assurance, Storrs, CT April 2015

Title: "Anti-reverse Engineering with Human-to-Device Authentication"

CHASE Workshop on Secure/Trustworthy Systems and Supply Chain Assurance, Storrs, CT April 2014

Title: "Design of Robust SRAM PUFs"

University of Connecticut (ECE Seminar Series), Storrs, CT December 2013

Title: "Trojan and Counterfeit Detection for Secure and Trustworthy Hardware"

Invited Panel and Roundtable Discussions (7)

Lead, **TAME Forum Breakout Session 3**, McLean, VA May 2018

Title: "National Technology Roadmap for Trusted and Assured Microelectronics"

Moderator, **HOST 2018 Visionary Panel**, McLean, VA May 2018

Title: "Future of HOST: What to Expect in the Next Decade? "

Panelist, **IEEE-HKN Student Leadership Conference**, Gainesville, FL April 2018

Title: "Life of a Research Professor"

Panelist, **EGN6933 - ENG FACULTY DEV**, Gainesville, FL January 2018

Title: "How to Get a Faculty Job"

Panelist, **Trusted Microelectronics Special Topic: Field Programmable Gate Array (FPGA) Assurance**, McLean, VA March 2017

Title: "FPGA Security Research Panel"

Moderator, **Dagstuhl Seminar 16202**, Wadern, Germany May 2016

Title: "PUFs and Security Components"

Panelist, **University of Maryland**, College Park, MD October 2013

Title: "6th Annual ECEGSA Roundtable on Academic Careers"

Tutorials (4)

International Test Conference (ITC) 2016 November 2015

Title: "Test Opportunities and Challenges for Secure Hardware and Verifying Trust in Integrated Circuits"

Presenters: D. Forte and S. Bhunia

International Test Conference (ITC) 2015 October 2015

Title: "Test Opportunities and Challenges for Secure Hardware and Verifying Trust in Integrated Circuits"

Presenters: M. Tehranipoor and D. Forte

Design Automation and Test in Europe (DATE) 2014 March 2014

Title: "All You Need to Know About Hardware Trojans and Counterfeit ICs"

Presenters: M. Tehranipoor and D. Forte

IEEE Conference on VLSI 2013 January 2014

Title: "All You Need to Know About Hardware Trojans and Counterfeit ICs"

Presenters: M. Tehranipoor and D. Forte

TEACHING EXPERIENCE

University of Florida, ECE Department, Gainesville, FL

Instructor

- EEL4310/5322: Digital Integrated Circuits Design/
VLSI Circuits and Technology S2017, S2018
- EEL6935: Advanced Hardware Security and Trust F2016, F2017

Co-Instructor

- EEL4930/5934: Introduction to Hardware Security and Trust S2016

University of Connecticut, ECE Department, Storrs, CT

Instructor

- ECE3421: VLSI Design and Simulation S2015
- ECE2001W: Electrical Circuits F2013, F2014
- ECE6095-005: Hardware Trojan Detection and Prevention S2014

Guest Lecturer

- ECE 4451/5451: Introduction to Hardware Security and Trust F2014

University of Maryland, ECE Department, College Park, MD

Co-instructor

- ENEE759T: Digital VLSI Design, Technology & Tools S2013

Teaching Assistant

- ENEE644: Computer-Aided Design of Digital System S2010
- ENEE350: Computer Organization F2007, S2007
- ENEE446: Digital Computer Design 2007
- ENEE241: Numerical Techniques in Engineering F2006

Mentor

- Teaching Assistant Training and Development (TATD) 2010–2011, 2011–2012

CITIZENSHIP STATUS

U.S. Citizen