Domenic J. Forte

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Research Interests

Counterfeit Electronic Component Detection and Avoidance: Includes physical inspection, electrical tests, and sensor design; provenance and supply chain tracking; from device level to system level
Physically Unclonable Functions (PUFs): Design, fabrication, and applications
Hardware Trojans: Pre-silicon prevention and post-silicon detection
Design Tools, Rules, Metrics, and Benchmarking: Hardware security assessment, mitigation, and obfuscation
Biometrics in IoT Applications: Includes emerging medico-chemical biometrics such as electrocardiogram (ECG) and photoplethysmograph (PPG)
PCB and IC Reverse and Anti-Reverse Engineering
Nanoscale Integration Challenges: 3D integration, thermal issues, security, and manufacturing variations in CMOS and beyond CMOS

Education

University of Maryland, College Park, MD
Ph.D., Electrical Engineering, August 2013

University of Maryland, College Park, MD
M.S., Electrical Engineering, December 2010

Manhattan College, Riverdale, NY
B.S., Electrical Engineering, *Summa Cum Laude*, May 2006

Professional Experience

University of Florida, ECE Department, Gainesville, FL
FICS Research Security and Assurance (SCAN) Lab Director, August 2016 – present
Assistant Professor, July 2015 – present

University of Connecticut, ECE Department, Storrs, CT
Assistant Professor, August 2013 – July 2015

University of Maryland, ECE Department, College Park, MD
Research Assistant, June 2009 – August 2013

University of Maryland, ECE Department, College Park, MD
Teaching Assistant, August 2006 – December 2010

National Institutes of Health CIT DCB CBEL SPIS, Bethesda, MD
Co-op Student Intern, June 2007 – May 2009

Maryland Engineering Research Internship Teams (MERIT), College Park, MD
REU Student, Summer 2005

Honors and Distinctions

- UF Provost's Excellence Award for Assistant Professors, 2017–2018
- ACM TODAES Best Paper Award, 2018
- NSF Faculty Early Career Development (CAREER) Award, 2017

- International Symposium for Testing and Failure Analysis (ISTFA) Outstanding Paper Award, 2017
- International Joint Conference on Biometrics (IJCB) Best Student Paper Award, 2017
- ACM Computing Reviews Notable Computing Books and Articles – 2016, Hardware Category
- Army Research Office (ARO) Young Investigator Award, 2016
- IEEE International Symposium on Hardware Oriented Security and Trust (HOST) Best Paper Award, 2016
- IEEE International Symposium on Hardware Oriented Security and Trust (HOST) Best Paper Nomination ($\times$2), 2016
- Schloss Dagstuhl - NSF Support Grant for Junior Researchers, Awarded, 2016
- IEEE International Symposium on Hardware Oriented Security and Trust (HOST) Best Paper Award, 2015
- Jacob K. Goldhaber Travel Award, University of Maryland, 2013
- Northrop Grumman Fellowship, 2012-2013 (Awarded to a top student in ECE)
- Design Automation Conference (DAC) Best Paper Nomination, 2012
- NASA/ESA Conference on Adaptive Hardware and Systems (AHS) Best Student Paper Award, 2011
- TA Teaching and Development (TATD) Fellow, University of Maryland, 2010–2011, 2011–2012
- George Corcoran Outstanding Teaching Award, University of Maryland, 2008 (Presented to two ECE graduate teaching assistants in 2008)
- Distinguished Teaching Assistant Award, University of Maryland, 2007-2008 (Awarded to top 10% of all graduate teaching assistants in the university)
- Co-recipient of medal for Electrical Engineering, Manhattan College, 2006 (Awarded at graduation to top two EE students in 2006)
- Next in Merit: Draddy Medal for General Excellence in Engineering, Manhattan College, 2006
- Society of Military Engineers (SAME) Scholarship, 2005
- Manhattan College Presidential Scholarship, 2002
- NY State Academic Excellence Scholarship, 2002

Awards Received by Student Advisees

- Ulbert (Joey) Botero: NSF Graduate Research Fellowship Program (GRFP), 2018
- Sreeja Chowdury: Three Minute Thesis (3MT) Competition Finalist at the University of Florida, 2018
- Sreeja Chowdury: ISC^2 Graduate Cybersecurity Scholarship, 2018
- Sreeja Chowdury: Awarded second place in poster competition at the Second Workshop for Women in Hardware and Systems Security (WISE), 2018
- Ulbert (Joey) Botero: Awarded best poster at FICS Research Annual Conference on Cybersecurity 2018
- Nima Karimian: Awarded best student paper at International Joint Conference on Biometrics (IJCB) 2017
- Zimu Guo: Awarded best demo at FICS Research Annual Conference on Cybersecurity 2017
- Sreeja Chowdury: Awarded best hardware primitive poster at FICS Research Annual Conference on Cybersecurity 2017
- Zimu Guo and Nima Karimian: Awarded best hardware security poster at FICS Research Annual Conference on Cybersecurity 2016

Books

B1. M. Tehranipoor, **D. Forte**, G. Rose, S. Bhunia, "Security Opportunities in Nano Devices and Emerging Technologies", CRC Press, 2017. *[Edited and Contributed]*

B2. **D. Forte**, S. Bhunia, M. Tehranipoor, "Hardware Protection through Obfuscation", Springer, 2017. *[Edited and Contributed]*

B3. M. Tehranipoor, U.J. Guin, **D. Forte**, "Counterfeit Integrated Circuits: Detection and Avoidance", Springer, 2015. *[Authored]*

Book Chapters

BC1. Q. Shi, **D. Forte**, M. Tehranipoor, "Deterrent Approaches Against Hardware Trojan Insertion," in The Hardware Trojan War by Swarup Bhunia, and Mark M. Tehranipoor, Springer, 2018.

BC2. F. Rahman, A. Nath, **D. Forte**, S. Bhunia, and M Tehranipoor, "Nano CMOS Logic-Based Security Primitive Design", in Security Opportunities in Nano Devices and Emerging Technologies by Mark M. Tehranipoor, Domenic Forte, Garrett Rose, and Swarup Bhunia, CRC Press, 2017.

BC3. H.T. Shen, F. Rahman, M. Tehranipoor, **D. Forte**, "Carbon-Based Novel Devices for Hardware Security", in Security Opportunities in Nano Devices and Emerging Technologies by Mark M. Tehranipoor, Domenic Forte, Garrett Rose, and Swarup Bhunia, CRC Press, 2017.

BC4. F. Rahman, A. Nath, S. Bhunia, **D. Forte**, M. Tehranipoor, "Composition of Physical Unclonable Functions: From Device to Architecture", in Security Opportunities in Nano Devices and Emerging Technologies by Mark M. Tehranipoor, Domenic Forte, Garrett Rose, and Swarup Bhunia, CRC Press, 2017.

BC5. B. Shakya, X. Xu, N. Asadi, M. Tehranipoor, **D. Forte**, "Leveraging Circuit Edit for Low-Volume Trusted Nanometer Fabrication", in Security Opportunities in Nano Devices and Emerging Technologies by Mark M. Tehranipoor, Domenic Forte, Garrett Rose, and Swarup Bhunia, CRC Press, 2017.

BC6. B. Shakya, M. Tehranipoor, S. Bhunia, **D. Forte**, "Introduction to Hardware Obfuscation: Motivation, Methods and Evaluation," in Hardware Protection through Obfuscation by Domenic Forte, Swarup Bhunia, and Mark M. Tehranipoor, Springer, 2017.

BC7. Z. Guo, M. Tehranipoor, **D. Forte**, "Permutation-Based Obfuscation," in Hardware Protection through Obfuscation by Domenic Forte, Swarup Bhunia, and Mark M. Tehranipoor, Springer, 2017.

BC8. M. T. Rahman, **D. Forte**, M. Tehranipoor, "Protection of Assets from Scan Chain Vulnerabilities through Obfuscation," in Hardware Protection through Obfuscation by Domenic Forte, Swarup Bhunia, and Mark M. Tehranipoor, Springer, 2017.

BC9. Q. Shi, K. Xiao, **D. Forte**, M. Tehranipoor, "Obfuscated Built-in Self Authentication," in Hardware Protection through Obfuscation by Domenic Forte, Swarup Bhunia, and Mark M. Tehranipoor, Springer, 2017.

BC10. A. Nahiyan, K. Xiao, **D. Forte**, M. Tehranipoor, "Security Rule Check," in Hardware IP Security and Trust by Prabhat Mishra, Swarup Bhunia and Mark Tehranipoor, Springer, 2017.

BC11. Q. Shi, **D. Forte**, M. Tehranipoor, "Analyzing Circuit Layout to Probing Attack," in Hardware IP Security and Trust by Prabhat Mishra, Swarup Bhunia and Mark Tehranipoor, Springer, 2017.

BC12. K. Xiao, **D. Forte**, M. Tehranipoor, "Circuit Timing Signature (CTS) for Detection of Counterfeit Integrated Circuits," in Secure System Design and Trustable Computing, by Chip Hong Chang and Miodrag Potkonjak, Springer, 2016.

Peer-Reviewed Journal Publications (accepted)

J1. K. Yang, U.J. Botero, H. Shen, D. Woodard, **D. Forte**, M. Tehranipoor, "UCR: An Unclonable Environmentally-Sensitive Chipless RFID Tag For Protecting Supply Chain", to appear *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, 2018.

J2. U.J. Botero, M. Tehranipoor, **D. Forte**, "Upgrade/Downgrade: Efficient and Secure Legacy Electronic System Replacement", *IEEE Design & Test*, 2018.

J3. Q. Shi , M. Tehranipoor, **D. Forte**, "Obfuscated Built-In Self-Authentication with Secure and Efficient Wire-Lifting", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2018.

J4. A. Nahiyan, F. Farahmandi, P. Mishra, **D. Forte**, M. Tehranipoor, "Security-aware FSM Design Flow for Identifying and Mitigating Vulnerabilities to Fault Attacks", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2018.

J5. X. Xu, S. Keshavarz, **D. Forte**, M. Tehranipoor, D.E. Holcomb, "Bimodal Oscillation as a Mechanism for Autonomous Majority Voting in PUFs", *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, Vol. 26, No. 11, November 2018.

J6. S. Amir, B. Shakya, X. Xu, Y. Jin, S. Bhunia, M. Tehranipoor, **D. Forte**, "Development and Evaluation of Hardware Obfuscation Benchmarks", *Journal of Hardware and Systems Security (HaSS)*, Vol. 2, No. 2, June 2018.

J7. Z. Guo, X. Xu, M. Tehranipoor, **D. Forte**, "SCARe: An SRAM-based Countermeasure Against IC Recycling Framework", *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, Vol. 26., No. 4, April 2018.

J8. M.M. Alam, S. Chowdhury, B. Park, D. Munzer, N. Maghari, M. Tehranipoor, **D. Forte**, "Challenges and Opportunities in Analog and Mixed Signal (AMS) Integrated Circuit (IC) Security", *Journal of Hardware and Systems Security (HaSS)*, Vol. 2, No. 1, March 2018.

J9. K. Yang, **D. Forte**, M. Tehranipoor, "ReSC: An RFID-Enabled Solution for Defending IoT Supply Chain", *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, Vol. 23, No. 3, February 2018.

J10. K. Yang, H. Shen, **D. Forte**, S. Bhunia, M. Tehranipoor, "Hardware-Enabled Pharmaceutical Supply Chain Security", *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, Vol. 23, No. 3, January 2018.

J11. F. Rahman, B. Shakya, Bicky, X. Xu, **D. Forte**, M. Tehranipoor,"Security Beyond CMOS: Fundamentals, Applications, and Roadmap", *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, Vol. 25, No. 12, December 2017.

J12. H. Shen, F. Rahman, B. Shakya, X. Xu, M. Tehranipoor, **D. Forte**,"Poly-Si Based Physical Unclonable Functions", *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, Vol. 25, No. 11, November 2017.

J13. E.L. Principe, N. Asadi, **D. Forte**, M. Tehranipoor, R. Chivas, M. DiBattista, S. Silverman, "Plasma FIB Deprocessing of Integrated Circuits from the Backside", *Electronic Device Failure Analysis (EDFA)*, Vol. 19, No. 4, November 2017.

J14. H. Wang, Q. Shi, **D. Forte**, M. Tehranipoor, "Probing Attacks on Integrated Circuits: Challenges and Research Opportunities", *IEEE Design & Test*, Vol. 34, No. 5, October 2017.

J15. M.T. Rahman, A. Hosey, Z. Guo, J. Carroll, **D. Forte**, M. Tehranipoor, "Systematic Correlation and Cell Neighborhood Analysis of SRAM-PUF for Robust and Unique Key Generation," *Journal of Hardware and Systems Security (HaSS)*, Vol. 1, No. 2, June 2017.

J16. N. Karimian, Z. Guo, M. Tehranipoor, **D. Forte**, "Highly Reliable Key Generation from Electrocardiogram (ECG)," *IEEE Transactions on Biomedical Engineering (TBME)*,Vol. 64, No. 6, June 2017.

J17. U.J. Guin, S. Bhunia, **D. Forte**, M. Tehranipoor, "SMA: A System-Level Mutual Authentication for Protecting Electronic Hardware and Firmware," *IEEE Transactions on Dependable and Secure Computing (TDSC)*, Vol. 14, No. 3, May-June 1 2017.

J18. Z. Guo, J. Di, M. Tehranipoor, **D. Forte**, "Obfuscation based Protection Framework Against Printed Circuit Boards Privacy Violation," *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, Vol. 22, No. 3, April 2017.

J19. K. Yang, **D. Forte**, M. Tehranipoor, "CDTA: A Comprehensive Solution for Counterfeit Detection, Traceability and Authentication in IoT Supply Chain," *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, Vol. 22, No. 3, April 2017.

J20. B. Shakya, T. He, H. Salmani, **D. Forte**, S. Bhunia, M. Tehranipoor, "Benchmarking of Hardware Trojans and Maliciously Affected Circuits", *Journal of Hardware and Systems Security (HaSS)*, Vol. 1, No. 1, April 2017.

J21. M. Alam, H. Shen, N. Asadi, M. Tehranipoor, **D. Forte**, "Impact of X-ray Tomography on the Reliability of Integrated Circuits", *IEEE Transactions on Device and Materials Reliability (TDMR)*, Vol. 17, No. 1, March 2017.

J22. N. Asadi, M. Tehranipoor, **D. Forte**, "PCB Reverse Engineering Using Non-destructive X-ray Tomography and Advanced Image Processing", *IEEE Transactions on Components, Packaging and Manufacturing (CPMT)*, Vol. 7, No. 2, February 2017.

J23. K. Xiao, **D. Forte**, Y. Jin, R. Karri, S. Bhunia, M. Tehranipoor, "Hardware Trojans: Lessons Learned After One Decade of Research", *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, Vol. 22, No. 1, June 2016. [**2018 ACM TODAES Best Paper, ACM Computing Reviews Notable Computing Books and Articles – 2016, Hardware Category**]

J24. U Guin, Q. Shi, **D. Forte**, M. Tehranipoor, "FORTIS: A Comprehensive Solution for Establishing Forward Trust for Protecting IPs and ICs," *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, Vol. 21, No. 4, June 2016

J25. U.J. Guin, **D. Forte**, M. Tehranipoor, "Design of Accurate Low-Cost On-Chip Structures for protecting Integrated Circuits against Recycling," *IEEE Transactions on VLSI Systems (TVLSI)*, Vol. 24, No. 4, April 2016.

J26. S. E. Quadir, J. Chen, **D. Forte**, N. Asadizanjani, S. Shahbazmohamadi, L. Wang, J. Chandy, M. Tehranipoor, "A Survey on Chip to System Reverse Engineering," *ACM Journal on Emerging Technologies in Computing Systems (JETC)*, Vol. 13, No. 1, April 2016.

J27. C. Bao, **D. Forte**, A. Srivastava, "On Reverse Engineering-Based Hardware Trojan Detection," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 35, No.1, January 2016

J28. C. Bao, **D. Forte**, A. Srivastava, "Temperature Tracking: Towards Robust Run-time Detection of Hardware Trojans," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)* Vol. 34, No. 10, October 2015.

J29. M.T. Rahman, F. Rahman, **D. Forte**, M. Tehranipoor, "An Aging-Resistant RO-PUF for Reliable Key Generation," *IEEE Transactions on Emerging Topics in Computing (TETC)*, September 2015.

J30. A. Mazady, M.T. Rahman, **D. Forte**, M. Anwar,"Memristor Nano-PUF A Security Primitive: Theory and Experiment," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS)*, Vol. 5, No. 2, June 2015.

J31. K. Xiao, **D. Forte**, M. Tehranipoor, "A Novel Built-In Self Authentication Technique to Prevent Inserting Hardware Trojans," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 32, No. 12, November 2014.

J32. **D. Forte** and A. Srivastava, "Improving the Quality of Delay-based PUFs via Optical Proximity Correction," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 32, No. 12, December 2013.

J33. **D. Forte** and A. Srivastava, "Thermal-Aware Sensor Scheduling for Distributed Estimation," *ACM Transactions on Sensor Networks (TOSN)*, Vol. 9, No. 4, July 2013.

J34. **D. Forte** and A. Srivastava, "Energy and Thermal-Aware Video Coding via Encoder/Decoder Workload Balancing", *IEEE Transactions on Embedded Computing Systems (TECS)*, Vol. 12, No. 2, May 2013.

J35. **D. Forte** and A. Srivastava, "Resource-Aware Architectures for Adaptive Particle Filter Based Visual Target Tracking", *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, Vol. 18, No. 2, April 2013.

Peer-Reviewed Conference/Workshop Publications

C1. A. Alaql, T. Hoque, **D. Forte**, S. Bhunia, "Quality Obfuscation for Reliable and Adaptive Hardware IP Protection", to appear IEEE VLSI Test Symposium (VTS), April 2019.

C2. Q. Shi, H. Wang, N. Asadi, M. Tehranipoor, **D. Forte**, "A Comprehensive Analysis on Vulnerability of Active Shields to Tilted Microprobing Attacks", to appear IEEE Asian Hardware-Oriented Security and Trust (AsianHOST), December 2018.

C3. A. Stern, U.J. Botero, B. Shakya, H. Shen, **D. Forte**, M. Tehranipoor, "EMFORCED: EM-based Fingerprinting Framework for Counterfeit Detection with Demonstration on Remarked ICs", to appear *IEEE International Test Conference (ITC)*, October-November 2018.

C4. H. Shen, N. Asadizanjani, M. Tehranipoor, **D. Forte**, "Nanopyramid: An Optical Scrambler Against Backside Probing Attacks", to appear *International Symposium for Testing and Failure Analysis (ISTFA)*, October 2018.

C5. P. Ghosh, **D. Forte**, D. Woodard, R.S. Chakraborty, "Automated Detection of Pin Defects on Counterfeit Microelectronics", to appear *International Symposium for Testing and Failure Analysis (ISTFA)*, October 2018.

C6. J. Park, X. Xu, Y. Jin, **D. Forte**, M. Tehranipoor, "Power-based Side-Channel Instruction-level Disassembler", *Design Automation Conference (DAC)*, June 2018.

C7. S. Chowdhury, X. Xu, M. Tehranipoor, **D. Forte**, "Aging Resistant RO PUF with Increased Reliability in FPGA", *International Conference on Reconfigurable Computing and FPGAs (ReConFig)*, December 2017.

C8. E.L. Principe, N.Asadizanjani, **D. Forte**, M. Tehranipoor, R. Chivas, M. DiBattista, S. Silverman, M. Marsh, N. Piche, J. Mastovich, "Steps Toward Automated Deprocessing of Integrated Circuits," *International Symposium for Testing and Failure Analysis (ISTFA)*, November 2017. [**ISTFA 2017 Outstanding Paper Award**]

C9. A. Chhotaray, A. Nahiyan, T. Shrimpton, **D. Forte**, M. Tehranipoor, "Standardizing Bad Cryptographic Practice - A Teardown of the IEEE Standard for Protecting Electronic-Design Intellectual Property," *ACM Conference on Computer and Communications Security (CCS)*, November 2017.

C10. Z. Guo, X. Xu, M. Tehranipoor, **D. Forte**, "MPA: Model-assisted PCB Attestation via Board-level RO and Temperature Compensation", *IEEE Asian Hardware-Oriented Security and Trust (AsianHOST)*, October 2017.

C11. K. Yang, U.J. Botero, H. Shen, **D. Forte**, M.Tehranipoor, "A Split Manufacturing Approach for Unclonable Chipless RFIDs for Pharmaceutical Supply Chain Security", *IEEE Asian Hardware-Oriented Security and Trust (AsianHOST)*, October 2017.

C12. A. Nahiyan, M. Sadi, R. Vittal, G. Contreras, **D. Forte**, M.Tehranipoor, "Hardware Trojan Detection through Information Flow Security Verification," *IEEE International Test Conference (ITC)*, October 2017.

C13. N. Karimian, D. Woodard, **D. Forte**, "On the Vulnerability of ECG Verification to Online Presentation Attacks," *IEEE International Joint Conference on Biometrics (IJCB)*, October 2017. **[IJCB 2017 Best Student Paper Award]**

C14. X. Xu, B. Shakya, M. Tehranipoor, **D. Forte**, "Novel Bypass Attack and BDD-based Tradeoff Analysis Against all Known Logic Locking Attacks," *International Conference on Cryptographic Hardware and Embedded Systems (CHES)*, September 2017.

C15. Z. Guo, X. Xu, M. Tehranipoor, **D. Forte**, "FFD: A Framework for Fake Flash Detection", *Design Automation Conference (DAC)*, June 2017.

C16. Q. Shi, K. Xiao, **D. Forte**, M. Tehranipoor, "Securing Split Manufactured ICs with Wire Lifting Obfuscated Built-In Self-Authentication", *GLSVLSI*, May 2017.

C17. S. Amir, B. Shakya, **D. Forte**, M. Tehranipoor, S. Bhunia, "Comparative Analysis of Hardware Obfuscation for IP Protection", *GLSVLSI*, May 2017.

C18. T. Byrant, S. Chowdhury, **D. Forte**, M. Tehranipoor, N. Maghari, "A Stochastic All-Digital Weak Physically Unclonable Function for Analog/Mixed-Signal Applications", *Hardware-Oriented Security and Trust (HOST)*, May 2017

C19. N. Karimian, F. Tehranipoor, Z. Guo, M. Tehranipoor, **D. Forte**, "Noise Assessment Framework for Optimizing ECG Key Generation", *IEEE International Conference on Technologies for Homeland Security (HST)*, April 2017.

C20. N. Karimian, Z. Guo, M. Tehranipoor, **D. Forte**, "Human Recognition from Photoplethysmography (PPG) Based on Non-fiducial Features", *IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP)*, March 2017.

C21. N. Karimian, M. Tehranipoor, **D. Forte**, "Non-Fiducial PPG-based Authentication for Healthcare Application", *International Conference on Biomedical and Health Informatics (BHI)*, February 2017.

C22. G. K. Contreras, A. Nahiyan, S. Bhunia, **D. Forte**, M. Tehranipoor, "Security Vulnerability Analysis of Design-for-Test Exploits for Asset Protection in SoCs," *Asia and South Pacific Design Automation Conference (ASP-DAC)*, January 2017.

C23. Z. Guo, M. Tehranipoor, **D. Forte**, "Aging Attacks for Key Extraction on Permutation-Based Obfuscation," *IEEE Asian Hardware-Oriented Security and Trust (AsianHOST)*, December 2016.

C24. T. Rahman, **D. Forte**, X. Wang, M. Tehranipoor, "Enhancing Noise Sensitivity of Embedded SRAMs for Robust True Random Number Generation in SoCs," *IEEE Asian Hardware-Oriented Security and Trust (AsianHOST)*, December 2016.

C25. M. M. Alam, M. Tehranipoor, **D. Forte** "Recycled FPGA Detection Using Exclusive LUT Path Delay Characterization," *IEEE International Test Conference (ITC)*, November 2016.

C26. B. Shakya, N. Asadi, **D. Forte**, M. Tehranipoor, "Chip Editor: Leveraging Circuit Edit for Logic Obfuscation and Trusted Fabrication," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, November 2016.

C27. Z. Guo, B. Shakya, H. Shen, S. Bhunia, N. Asadizanjani, **D. Forte**, M. Tehranipoor, "A New Methodology to Protect PCBs from Non-destructive Reverse Engineering", *International Symposium for Testing and Failure Analysis (ISTFA)*, November 2016.

C28. N. Asadizanjani, **D. Forte**, M. Tehranipoor, "Non-destructive Bond Pull and Ball Shear Failure Analysis Based on Real Structural Properties" *International Symposium for Testing and Failure Analysis (ISTFA)*, November 2016.

C29. N. Asadizanjani, S. Gattigowda, N. Dunn, M. Tehranipoor, **D. Forte**, "A Database for Counterfeit Electronics and Automatic Defect Detection Based on Image Processing and Machine Learning," *International Symposium for Testing and Failure Analysis (ISTFA)*, November 2016.

C30. T. Bryant, S. Chowdhury, **D. Forte**, M. Tehranipoor, N. Maghari, "A Stochastic Approach to Analog Physical Unclonable Function," *IEEE Midwest Symposium on Circuits and Systems (MWSCAS)*, October 2016.

C31. N. Karimian, M. Tehranipoor, D. Woodard, **D. Forte**, "Biometrics for Authentication in Resource-Constrained Systems," *International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC)*, August 2016.

C32. H. Shen, F. Rahman, B. Shakya, M. Tehranipoor, **D. Forte**,"Selective Enhancement of Randomness at the Materials Level: Poly-Si Based Physical Unclonable Functions (PUFs)", *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, July 2016.

C33. A. Nahiyan, K. Xiao, K. Yang, Y. Jin, **D. Forte**, M. Tehranipoor, "AVFSM: A Framework for Identifying and Mitigating Vulnerabilities in FSMs", *Design Automation Conference (DAC)*, June 2016.

C34. Z. Guo, N. Karimian, M. Tehranipoor, **D. Forte**, "Hardware Security Meets Biometrics for the Age of IoT", *IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2016.

C35. T. Le, J. Di, M. Tehranipoor, **D. Forte**, L. Wang, "Tracking Data Flow at Gate-Level through Structural Checking", *GLSVLSI*, May 2016.

C36. Q. Shi, N. Asadizanjani, **D. Forte**, M.Tehranipoor, "A Layout-driven Framework to Assess Vulnerability of ICs to Microprobing Attacks", *Hardware-Oriented Security and Trust (HOST)*, May 2016. **[HOST 2016 Best Paper Award]**

C37. Z. Guo, M. T. Rahman, M. Tehranipoor, **D. Forte**, "A Zero-cost Approach to Detect Recycled SoCs Using Embedded SRAM", *Hardware-Oriented Security and Trust (HOST)*, May 2016.

C38. K. Yang, **D. Forte**, M. Tehranipoor, "UCR: Unclonable Chipless RFID Tag", *Hardware-Oriented Security and Trust (HOST)*, May 2016. **[HOST 2016 Best Paper Nomination]**

C39. F. Rahman, **D. Forte**, and Mark Tehranipoor, "Reliability vs. Security: Challenges and Opportunities for Developing Reliable and Secure Integrated Circuits," *International Reliability Physics Symposium (IRPS)*, April 2016

C40. B. Shakya, F. Rahman, M. Tehranipoor, **D. Forte**, "Harnessing Nanoscale Device Properties for Hardware Security", *Microprocessor Test and Verification (MTV)*, December 2015.

C41. K. Yang, **D. Forte**, and M. Tehranipoor, "Protecting Endpoint Devices in IoT Supply Chain", *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, November 2015.

C42. H. Dogan, M. Alam, N. Asadizanjani, S. Shahbazmohamadi, **D. Forte**, and M. Tehranipoor, "Analyzing the Impact of X-ray Tomography for Non-destructive Counterfeit Detection", *International Symposium for Testing and Failure Analysis (ISTFA)*, November 2015.

C43. N. Asadizanjani, S. Shahbazmohamadi, M. Tehranipoor, **D. Forte** "Non-destructive PCB Reverse Engineering Using X-ray Micro Computed Tomography", *International Symposium for Testing and Failure Analysis (ISTFA)*, November 2015.

C44. B. Shakya, U. Guin, M. Tehranipoor, **D. Forte**, "Performance Optimization for On-Chip Sensors to Detect Recycled ICs," *IEEE International Conference on Computer Design (ICCD)*, October 2015.

C45. M. T. Rahman, **D. Forte**, F. Rahman, M. Tehranipoor, "A Pair Selection Algorithm for Robust RO-PUF Against Environmental Variations and Aging," *IEEE International Conference on Computer Design (ICCD)*, October 2015.

C46. S. Chen, J. Chen, **D. Forte**, J. Di, M. Tehranipoor, L. Wang, "Chip-level Anti-reverse Engineering using Transformable Interconnects," *IEEE Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT)*, October 2015.

C47. K. Yang, **D. Forte**, M.Tehranipoor, "ReSC: RFID-enabled Supply Chain Management and Traceability for Network Devices," *11th Workshop on RFID Security (RFIDSec 2015)*, June 2015.

C48. Z. Guo, J. Di, M. Tehranipoor, **D. Forte**, "Investigation of Obfuscation-based Anti-Reverse Engineering for Printed Circuit Boards," *Design Automation Conference (DAC) 2015*, June 2015.

C49. K. Xiao, **D. Forte**, M. Tehranipoor, "Efficient and Secure Split Manufacturing via Obfuscated Built-In Self-Authentication," *Hardware-Oriented Security and Trust (HOST) 2015*, May 2015. **[HOST 2015 Best Paper Award]**

C50. N. Karimian, F. Tehranipoor, M.T. Rahman, **D. Forte**, "Genetic Algorithm for Hardware Trojan Detection with Ring Oscillator Network (RON)" in *IEEE International Conference on Technologies for Homeland Security (HST)*, April 2015.

C51. K. Yang, **D. Forte**, M. Tehranipoor, "An RFID-based Technology for Electronic Component and System Counterfeit Detection and Traceability" in *IEEE International Conference on Technologies for Homeland Security (HST)*, April 2015.

C52. A. Hosey, M.T. Rahman, K. Xiao, **D. Forte**, M. Tehranipoor, "Advanced Analysis of Cell Stability for Reliable SRAM PUF," IEEE Asian Test Symposium (ATS), November 2014.

C53. S. Shahbazmohamadi, **D. Forte**, M. Tehranipoor, "Advanced Physical Inspection Methods for Counterfeit Detection", *International Symposium for Testing and Failure Analysis (ISTFA)*, November 2014.

C54. M.T. Rahman, **D. Forte**, Q. Shi, G. Contreras, M. Tehranipoor, "CSST: Preventing Distribution of Unlicensed and Rejected ICs by Untrusted Foundry and Assembly," *IEEE Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT)*, October 2014.

C55. H. Dogan, **D. Forte**, M. Tehranipoor, "Aging Analysis for Recycled FPGA Detection," *IEEE Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT)*, October 2014.

C56. U. Guin, X. Zhang, **D. Forte**, M. Tehranipoor, "Low-cost On-Chip Structures for Combating Die and IC Recycling," *Design Automation Conference (DAC)*, June 2014.

C57. M.T. Rahman, K. Xiao, X. Zhang, **D. Forte**, Z. Shi, M. Tehranipoor, "TI-TRNG: Technology Independent True Random Number Generator," *Design Automation Conference (DAC)*, June 2014.

C58. M.T. Rahman, **D. Forte**, Q. Shi, G. Contreras, M. Tehranipoor, "CSST: An Efficient Secure Split-Test for Preventing IC Piracy," in IEEE North Atlantic Test Workshop (NATW), May 2014

C59. K. Xiao, M.T. Rahman, **D. Forte**, M. Su, Y. Huang, M.Tehranipoor, "Bit Selection Algorithm Suitable for High-Volume Production of SRAM-PUF," Hardware-Oriented Security and Trust (HOST), May 2014.

C60. C. Bao, **D. Forte**, A. Srivastava, "On Application of One-class SVM to Reverse Engineering-Based Hardware Trojan Detection", in *International Symposium on Quality Electronic Design (ISQED)*, March 2014.

C61. M.T. Rahman, **D. Forte**, J. Fahrny, M. Tehranipoor, "ARO-PUF: An Aging-Resistant Ring Oscillator PUF Design", in *Design, Automation, and Test in Europe (DATE)*, March 2014.

C62. U. Guin, **D. Forte**, M. Tehranipoor, "Anti-Counterfeit Techniques: From Design to Resign", in *Microprocessor Test and Verification (MTV)*, December 2013.

C63. **D. Forte**, C. Bao, A. Srivastava, "Temperature Tracking: An Innovative Run-Time Approach for Hardware Trojan Detection", *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, November 2013.

C64. **D. Forte** and A. Srivastava, "Manipulating Manufacturing Variations for Better Silicon-Based Physically Unclonable Functions", *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, August 2012.

C65. **D. Forte** and A. Srivastava, "On Improving the Uniqueness of Silicon-Based Physically Unclonable Functions Via Optical Proximity Correction", *Design Automation Conference (DAC)*, June 2012. [**DAC-2012 Best Paper Nomination**]

C66. **D. Forte** and A. Srivastava, "Adaptable Architectures for Distributed Visual Target Tracking", *IEEE International Conference on Computer Design (ICCD)*, October 2011.

C67. **D. Forte** and A. Srivastava, "Energy-Aware and Quality-Scalable Data Placement and Retrieval for Disks in Video Server Environments", *IEEE International Conference on Computer Design (ICCD)*, October 2011.

C68. **D. Forte** and A. Srivastava, "Energy-aware video storage and retrieval in server environments," *International Green Computing Conference and Workshops (IGCC)*, July 2011.

C69. **D. Forte** and A. Srivastava, "Resource-aware architectures for particle filter based visual target tracking," *International Green Computing Conference and Workshops (IGCC)*, July 2011.

C70. **D. Forte** and A. Srivastava, "Adaptable video compression and transmission using lossy and workload balancing techniques", *NASA/ESA Conference on Adaptive Hardware and Systems (AHS)*, June 2011. [**Awarded AHS-2011 Best Student Paper**]

C71. **D. Forte** and A. Srivastava, "Energy-aware video coding of multiple views via workload balancing", *NASA/ESA Conference on Adaptive Hardware and Systems (AHS)*, June 2011.

C72. **D. Forte** and A. Srivastava, "Energy and Thermal-Aware Video Coding via Encoder/Decoder Workload Balancing", *International Symposium on Low Power Electronics and Design (ISLPED)*, August 2010.

C73. **D. Forte** and A. Srivastava, "Thermal-Aware Sensor Scheduling for Distributed Estimation", *International Conference on Distributed Computing in Sensor Systems (DCOSS)*, June 2010.

Non-Refereed Conference Papers

CP1. D. Koblah, U.J. Botero, N. Asadi, D. Woodard, **D. Forte**, "Targeted Via Modeling in Printed Circuit Boards Using a Convolutional Neural Network", in *GOMACTech*, March 2019.

CP2. A. Stern, K. Yang, J. Vosatka, A. Duncan, J. Park, **D. Forte**, M. Tehranipoor, "RASC: Enabling Remote Access to Side-Channels for Mission Critical Systems", in *GOMACTech*, March 2019.

CP3. H. Wang, Q. Shi, N. Asadi, **D. Forte**, M. Tehranipoor, "A Physical Design Flow against Front-side Probing Attacks by Internal Shielding", in *SRC TECHCON*, September 2018.

CP4. E.L. Principe, N. Asadi, **D. Forte**, M. Tehranipoor, M. DiBattista, R. Chivas, S. Silverman, N. Piche, M. Marsh, J. Mastovich, "Steps Toward Computational Guided Deprocessing of Integrated Circuits" in *GOMACTech*, March 2018.

CP5. D. Capecci, G. Contreras, **D. Forte**, M.Tehranipoor, S. Bhunia, "Automated SoC Security from Design to Fabrication" in *GOMACTech*, March 2018.

CP6. S. Baireddy, U.J. Botero, N. Asadi, M.Tehranipoor, D. Woodard, **D. Forte**, "Automated Detection of Counterfeit IC Defects Using Image Processing" in *GOMACTech*, March 2018.

CP7. U.J. Botero, M.Tehranipoor, **D. Forte**, "Downgrade: A Framework for Obsolescence Handling through Backwards Compatibility" in *GOMACTech*, March 2018.

CP8. Z. Guo, M. Tehranipoor, **D. Forte**, "Memory-based Counterfeit IC Detection Framework", *SRC TECHCON*, September 2017.

CP9. Q. Shi, N. Asadizanjani, **D. Forte**, M.Tehranipoor, "Layout-based Microprobing Vulnerability Assessment for Security Critical Applications," in *GOMACTech*, March 2017.

CP10. M. T. Rahman, **D. Forte**, and M. Tehranipoor, "SRAM Inspired Design and Optimization for Developing Robust Security Primitives," in *SRC TECHCON*, September 2016. [**Awarded Best in Session**]

CP11. M. M. Alam, N. Asadizanjani, M.Tehranipoor, **D. Forte**, "The Impact of X-ray Tomography on the Reliability of FPGAs " in *GOMACTech*, March 2016.

CP12. Z. Guo, N. Karimian, M. Tehranipoor, **D. Forte**, "Biometric Based Human-to-Device (H2D) Authentication", in *GOMACTech*, March 2016.

CP13. N. Asadizanjani, S. Shahbazmohamadi, **D. Forte**, M. Tehranipoor, "Nondestructive X-ray Tomography Based Bond Pull and Ball Shear Analysis" in *GOMACTech*, March 2016.

CP14. M. T. Rahman, **D. Forte**, and M. Tehranipoor, "Robust SRAM-PUF: Cell Stability Analysis and Novel Bit-Selection Algorithm," *SRC TECHCON*, September 2015.

CP15. M.T. Rahman, A. Hosey, F. Rahman, **D. Forte**, M. Tehranipoor, "RePa: A Pair Selection Algorithm for Reliable Keys from RO-based PUF" in *GOMACTech*, March 2015.

CP16. H. Dogan, **D. Forte**, M. Tehranipoor, "Aging Analysis for Recycled FPGA Detection" in *GOMACTech*, March 2015.

CP17. N. Asadizanjani, S. E. Quadir, S. Shahbazmohamadi, M. Tehranipoor, **D. Forte**, "Rapid Non-destructive Reverse Engineering of Printed Circuit Boards by High Resolution X-ray Tomography" in *GOMACTech*, March 2015.

CP18. U. Guin, **D. Forte**, M. Tehranipoor, "Low-cost On-Chip Structures for Combatting Die and IC Recycling," in *GOMACTech*, March 2014.

CP19. K. Xiao, M.T. Rahman, **D. Forte**, M. Tehranipoor, "Low-cost Analysis for Identification of Mass-Produced Electronic Devices," in *GOMACTech*, March 2014.

CP20. U. Guin, **D. Forte**, D. DiMase, M. Tehranipoor, "Counterfeit IC Detection: Test Method Selection Considering Test Time, Cost, and Tier Level Risks," in *GOMACTech*, March 2014.

Patents

Pt1. S. Bhunia, H. Shen, M. Tehranipoor, **D. Forte**, N. Asadizanjani, *Vanishing via for hardware IP protection from reverse engineering*, filed January 2018.

Pt2. M. Tehranipoor, **D. Forte**, N. Asadizanjani, Q. Shi, *Layout-Driven Method to Assess Vulnerability of ICs To Microprobing Attacks*, filed December 2017.

Pt3. M. Tehranipoor, K. Yang, H. Shen, **D. Forte**, *UCR: An Unclonable Environmentally-Sensitive Chipless RFID Tag*, filed October 2017.

Pt4. M. Tehranipoor, **D. Forte**, B. Shakya, N. Asadizanjani, *Circuit Edit and Obfuscation for Trusted Chip Fabrication*, filed June 2017.

Pt5. M. Tehranipoor, U. Guin, **D. Forte**, *A Comprehensive Framework for Protecting Intellectual Property in Semiconductor Industry*, filed June 2017.

Advisees

Current Post-doctoral Fellows and Research Scientists[1]

Fatemah Ganji, Haoting Shen*, Qihang Shi*, Shahin Tajik*

[1]Note: $\star$ and † indicate co-advised by Mark Tehranipoor and Swarup Bhunia respectively

Past Post-doctoral Fellows and Research Scientists (Title and Current Affiliation)

Navid Asadi* (Assistant Professor, University of Florida), Xiaolin Xu* (Assistant Professor, University of Illinois at Chicago), Jungmin Park*† (Research Assistant Professor, University of Florida)

Current PhD

Bicky Shakya, Mahbub Alam, Sreeja Chowdhury, Sarah Amir, Ulbert (Joey) Botero, Sumaiya (Joyti) Shomaji, Muhtadi (Zaki) Choudhury, Rabin Acharya,

Past PhD (Title and Current Affiliation)

University of Florida: Zimu Guo (Micron Technology)
University of Connecticut: Nima Karimian (Assistant Professor, San Jose State University)

Past MS

University of Florida: Bicky Shakya, Rahul Vittal, Janani Prakash
University of Connecticut: Nima Karimianbahnemiri

Past Visting MS (Institution)

Pallabi Ghosh (IIT Kharagpur)

Current Undergrad

David Koblah, James Mashburn

Past Undergrad

Sriram Baireddy, Jackson Carroll, Julia Merino-Calleja, Andrew Stern, Nathan Dunn*, Somtochukwu Okwuosah, Alison Hosey, Jacquelyn Khadijah-Hajdu*, Wesley Stevens*, Ryan Nesbit*, Dan Guerrera*, Shane Tobey*, Kasim Ward*, Carl DiFrederico*, Anthony Schend*, Michael Vetri*, Tyler Rich*

Professional Activities

Editorial Activities

Associate Editor, Springer Journal of Hardware and System Security (HaSS), 2016–present
Guest Editor, Springer Journal of Hardware and System Security (HaSS) Special Issue on "Hardware Reverse Engineering and Obfuscation", 2018
Guest Editor, IEEE Computer Special Issue on "Supply Chain Security for Cyber-Infrastructure", 2016

Conference Organizing Committee

Program Chair, International Symposium on Hardware-Oriented Security and Trust (HOST), 2019
Publicity Chair, IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2019
Vice Program Chair, International Symposium on Hardware-Oriented Security and Trust (HOST), 2018
Reverse Engineering Track Chair, International Symposium for Testing and Failure Analysis (ISTFA), 2018
Publicity Chair, Workshop on Attacks and Solutions in Hardware Security (ASHES), 2018
Publicity Chair, IEEE Asian Hardware-Oriented Security and Trust Symposium (AsianHOST), 2016–2018
Program Co-Chair, International Verification and Security Workshop (IVSW), 2017
Tutorial Chair, International Symposium on Hardware-Oriented Security and Trust (HOST), 2017
Poster Chair, FICS Research Annual Conference on Cybersecurity, 2017
Reverse Engineering Track Chair, International Symposium for Testing and Failure Analysis (ISTFA), 2016
Publicity Chair, International Symposium on Hardware-Oriented Security and Trust (HOST),

2015, 2016
Hardware Security Challenge Co-Chair, CSI Cybersecurity, Education & Diversity Challenge Week (CyberSEED), 2014

Program Committee (PC)

2019: Great Lakes Symposium on VLSI (GLSVLSI)

2018: Asian Hardware Oriented Security and Trust Symposium (AsianHOST), DAC PhD Forum, Great Lakes Symposium on VLSI (GLSVLSI), International Symposium on Quality Electronic Design (ISQED), International Symposium on Hardware-Oriented Security and Trust (HOST), International Symposium for Testing and Failure Analysis (ISTFA), International Test Conference (ITC), International Workshop on Physical Attacks and Inspection on Electronics (PAINE), Network and Distributed System Security Symposium (NDSS), Smart Card Research and Advanced Application Conference (CARDIS), Workshop on Attacks and Solutions in Hardware Security (ASHES)

2017: Asian Hardware Oriented Security and Trust Symposium (AsianHOST), DAC PhD Forum, Great Lakes Symposium on VLSI (GLSVLSI), International Conference on Computer-Aided Design (ICCAD), International Symposium on Hardware-Oriented Security and Trust (HOST), International Symposium on Quality Electronic Design (ISQED), International Test Conference (ITC), Network and Distributed System Security Symposium (NDSS), Smart Card Research and Advanced Application Conference (CARDIS), Workshop on Attacks and Solutions in Hardware Security (ASHES)

2016: Asian Hardware Oriented Security and Trust Symposium (AsianHOST), Design Automation Conference (DAC), DAC PhD Forum, International Symposium on Hardware-Oriented Security and Trust (HOST), International Conference on Computer-Aided Design (ICCAD), International Symposium on Quality Electronic Design (ISQED), International Symposium for Testing and Failure Analysis (ISTFA)

2015: Design Automation Conference (DAC), International Conference on Computer-Aided Design (ICCAD), International Conference on Computer Design (ICCD), International Symposium on Hardware-Oriented Security and Trust (HOST), International Test Conference (ITC), International Symposium on Quality Electronic Design (ISQED), Workshop on Embedded Systems Security (WESS)

2014: International Symposium on Hardware-Oriented Security and Trust (HOST), TRUDEVICE Workshop on Test and Fault Tolerance for Secure Devices, Workshop on Embedded Systems Security (WESS)

2013: Workshop on Embedded Systems Security (WESS)

Working Groups

2018–present: IEEE P1735 Working Group, Member
2018–present: TAME Hardware Vulnerability Database Working Group, Scribe and Member

Proposal Panelist/Reviewer

2018: National Science Foundation (NSF), Critical Infrastructure Resilience Institute (CIRI)
2017: American Association for the Advancement of Science (AAAS), Army Research Office (ARO)
2016: National Science Foundation (NSF)

Reviewer for

ACM Journal on Emerging Technologies in Computing Systems (JETC), 2015
ACM Transactions on Design Automation of Electronic Systems (TODAES), 2014-2016
ACM Transactions on Privacy and Security (TOPS), 2017
IEEE Access, 2015
IEEE Communications Letters, 2014
IEEE Design & Test, 2014

IEEE Journal of Solid-State Circuits, 2018
IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS), 2015
Transactions on Biomedical Engineering (TBME), 2018
IEEE Transactions on Circuits and Systems I (TCAS1), 2014-2017
IEEE Transactions on Circuits and Systems II (TCAS2), 2014
IEEE Transactions on Computer-Aided Design of Integrated Circuits (TCAD), 2014, 2016-2017
IEEE Transactions on Computers, 2015-2017
IEEE Transactions on Embedded Computing Systems (TECS), 2016
IEEE Transactions on Emerging Topics in Computing (TETC), 2013, 2015
IEEE Transactions on Industrial Electronics (TIE), 2018
IEEE Transactions on Information Forensics and Security (TIFS), 2014-2017
IEEE Transactions on Multi-Scale Computing Systems (TMSCS), 2015
IEEE Transactions on Nanotechnology (TNANO), 2015
IEEE Transactions on Dependable and Secure Computing (TDSC), 2017
IEEE Transactions on VLSI Systems (TVLSI), 2013-2018
IET Computers & Digital Techniques, 2014
Image and Vision Computing, 2017
Journal of Electronic Testing: Theory and Applications (JETTA), 2016

Departmental Appointments

University of Florida, ECE Department, Gainesville, Fl

Faculty Search Committee, AY 2017-2018
Graduate Recruiting & Admissions Committee (GRAC), AY 2015-2016, AY 2016-2017, AY 2017-2018
EEL 3111 Circuits 1 ABET Course Committee, AY 2015-2016, AY 2016-2017
EEE 4310 Digital Integrated Circuits ABET Course Committee, AY 2015-2016, AY 2016-2017, AY 2017-2018
EEE 4404 Mixed Signal IC Testing I ABET Course Committee, AY 2016-2017, AY 2017-2018
EEL 4242 Power Electronics 1 ABET Course Committee, AY 2017-2018

University of Connecticut, ECE Department, Storrs, CT

Department Judge- First Annual Graduate Poster Competition, 2015
Course and Curriculum Committee, AY 2014-2015

Invited Talks (16)

NXP Semiconductors, Chandler, AZ October 2018
Title: "CAD Assessment and Flow for Protection Against Chip Editing and Probing"

CIA Summer Symposium, McLean, VA June 2018
Title: "Biometrics Research at the University of Florida"

International Test & Evaluation Association 2018 Cybersecurity Workshop, Fort Walton Beach, FL March 2018
Title: "Hardware for Cyber (H4C): A Suite of Electronic System Protections from Nano to System Levels"

CIA Tech Exchange on Trust & Validation of Electronics, Chantilly, VA Feb. 2018
Title: "Trust & Validation of Electronics at FICS Research"

Cisco Research Center System and Platform Security PI Summit, San Jose, CA Dec. 2017
Title: "Teardown and Recommendations for IEEE Standard for Protecting Electronic-Design Intellectual Property"

International Test Conference (ITC) 2017, Fort Worth, TX Nov. 2017
Title: "Upgrade/Downgrade: A Perspective on Challenges and Opportunities in Overcoming the Legacy System Issue"

AsianHOST 2017, Beijing, China Oct. 2017

Title: "Security of the Internet of Things: New Frontiers"

GRC Technology Transfer e-Workshop, WebEx July 2016
Title: "Design of Low-Cost Memory-Based Security Primitives and Techniques for High-Volume Products"

Workshop on Cyber Science, Biometrics and Digital Forensics, Miami, FL November 2015
Title: "Biometrics Meets Hardware Security"

Northrop Grumman Lunch N Learn, Baltimore, MD November 2015
Title: "New Directions in Hardware Security and Supply Chain Assurance"

Workshop on Cryptography and Hardware Security for the Internet of Things, College Park, MD October 2015
Title: "Hardware Security Challenges and Solutions in the IoT Era"

University of Florida, Gainesville, FL March 2015
Title: "Hardware-based Primitives for System Authentication and Protection"

Design, Automation & Test in Europe (DATE), Dresden, DE March 2014
Title: "Protocol Attacks on Advanced PUF Protocols and Countermeasures"

University of South Florida, Tampa, FL March 2013
Title: "Towards Comprehensive Solutions for Hardware Security"

Raytheon BBN Technologies, Columbia, MD March 2013
Title: "Towards Comprehensive Solutions for Hardware Security"

University of Connecticut, Storrs, CT February 2013
Title: "Towards Comprehensive Solutions for Hardware Security"

Campus and Departmental Talks (6)

Forum on Trusted and Assured MicroElectronics (TAME), Gainesville, FL November 2017
Title: "Emerging Solutions for Trusted and Assured Microelectronics"

UF Eta Kappa Nu (HKN) Speaker Series, Gainesville, FL November 2017
Title: "Introduction to FICS Research"

FICS Annual Conference on Cybersecurity, Gainesville, FL February 2016
Title: "Human-to-Device Authentication"

CHASE Conference on Secure/Trustworthy Systems and Supply Chain Assurance, Storrs, CT April 2015
Title: "Anti-reverse Engineering with Human-to-Device Authentication"

CHASE Workshop on Secure/Trustworthy Systems and Supply Chain Assurance, Storrs, CT April 2014
Title: "Design of Robust SRAM PUFs"

University of Connecticut (ECE Seminar Series), Storrs, CT December 2013
Title: "Trojan and Counterfeit Detection for Secure and Trustworthy Hardware"

Invited Panel and Roundtable Discussions (9)

Panelist, **University of Maryland**, College Park, MD November 2018
Title: "11th Annual ECEGSA Roundtable on Academic Careers"

Panelist, **IEEE International Workshop on Physical Attacks And Inspection On Electronics (PAINE)**, San Francisco, CA June 2018
Title: "Crossroad Between Physical Inspection and Hardware Security"

Lead, **TAME Forum Breakout Session 3**, McLean, VA May 2018
Title: "National Technology Roadmap for Trusted and Assured Microelectronics"

Moderator and Organizer, **HOST 2018 Visionary Panel**, McLean, VA May 2018
Title: "Future of HOST: What to Expect in the Next Decade?"

Panelist, **IEEE-HKN Student Leadership Conference**, Gainesville, FL April 2018
Title: "Life of a Research Professor"

Panelist, **EGN6933 - ENG FACULTY DEV**, Gainesville, FL January 2018
Title: "How to Get a Faculty Job"

Panelist, **Trusted Microelectronics Special Topic: Field Programmable Gate Array (FPGA) Assurance**, McLean, VA March 2017
Title: "FPGA Security Research Panel"

Moderator, **Dagstuhl Seminar 16202**, Wadern, Germany May 2016
Title: "PUFs and Security Components"

Panelist, **University of Maryland**, College Park, MD October 2013
Title: "6th Annual ECEGSA Roundtable on Academic Careers"

Tutorials (5)

Conference on Cryptographic Hardware and Embedded Systems (CHES) 2018 September 2018
Title: "Counterfeit Integrated Circuits: Threats, Detection, and Avoidance"
Presenters: D. Forte and R.S. Chakraborty

International Test Conference (ITC) 2016 November 2015
Title: "Test Opportunities and Challenges for Secure Hardware and Verifying Trust in Integrated Circuits"
Presenters: D. Forte and S. Bhunia

International Test Conference (ITC) 2015 October 2015
Title: "Test Opportunities and Challenges for Secure Hardware and Verifying Trust in Integrated Circuits"
Presenters: M. Tehranipoor and D. Forte

Design Automation and Test in Europe (DATE) 2014 March 2014
Title: "All You Need to Know About Hardware Trojans and Counterfeit ICs"
Presenters: M. Tehranipoor and D. Forte

IEEE Conference on VLSI 2013 January 2014
Title: "All You Need to Know About Hardware Trojans and Counterfeit ICs"
Presenters: M. Tehranipoor and D. Forte

Teaching Experience

University of Florida, ECE Department, Gainesville, FL

Instructor

- EEL4310/5322: Digital Integrated Circuits Design/ VLSI Circuits and Technology S'17–S'19
- EEE6742 (Formerly EEL6935): Advanced Hardware Security and Trust F'16–F'18

Co-Instructor

- EEL4930/5934: Introduction to Hardware Security and Trust S'16

University of Connecticut, ECE Department, Storrs, CT

Instructor

- ECE3421: VLSI Design and Simulation S'15
- ECE2001W: Electrical Circuits F'13, F'14
- ECE6095-005: Hardware Trojan Detection and Prevention S'14

Guest Lecturer

- ECE4451/5451: Introduction to Hardware Security and Trust F'14

University of Maryland, ECE Department, College Park, MD

Co-instructor

- ENEE759T: Digital VLSI Design, Technology & Tools — S'13

Teaching Assistant

- ENEE644: Computer-Aided Design of Digital System — S'10
- ENEE350: Computer Organization — F'07, S'07
- ENEE446: Digital Computer Design — F'07
- ENEE241: Numerical Techniques in Engineering — F'06

Note: 'F' and 'S' denote Fall and Spring respectively.

Mentor

- Teaching Assistant Training and Development (TATD) — 2010–2011, 2011–2012

Citizenship Status

U. S. Citizen